



CY62147G/CY621472G

MoBL<sup>®</sup> Automotive

## 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

### Features

- High speed: 45 ns/55 ns
- Temperature Ranges
  - Automotive-A: -40 °C to +85 °C
  - Automotive-E: -40 °C to +125 °C
- Ultra-low standby power
  - Typical standby current: 3.5 μA
- Embedded ECC for single-bit error correction<sup>[1]</sup>
- Wide voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 48-ball VFBGA and 44-pin TSOP II packages

### Functional Description

CY62147G/CY621472G is high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. Both devices are offered in single and dual chip enable options and in multiple pin configurations.

Devices with a single chip enable input are accessed by asserting the chip enable ( $\overline{CE}$ ) input LOW. Dual chip enable devices are accessed by asserting both chip enable inputs –  $\overline{CE}_1$  as low and  $CE_2$  as HIGH.

Data writes are performed by asserting the Write Enable ( $\overline{WE}$ ) input LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>15</sub> and address on A<sub>0</sub> through A<sub>17</sub> pins. The Byte High Enable ( $\overline{BHE}$ ) and Byte Low Enable ( $\overline{BLE}$ ) inputs control write operations to the upper and lower bytes of the specified memory location.  $\overline{BHE}$  controls I/O<sub>8</sub> through I/O<sub>15</sub> and  $\overline{BLE}$  controls I/O<sub>0</sub> through I/O<sub>7</sub>.

Data reads are performed by asserting the Output Enable ( $\overline{OE}$ ) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). Byte accesses can be performed by asserting the required byte enable signal ( $\overline{BHE}$  or  $\overline{BLE}$ ) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a HI-Z state when the device is deselected ( $\overline{CE}$  HIGH for a single chip enable device and  $\overline{CE}_1$  HIGH/ $CE_2$  LOW for a dual chip enable device), or control signals are deasserted ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ).

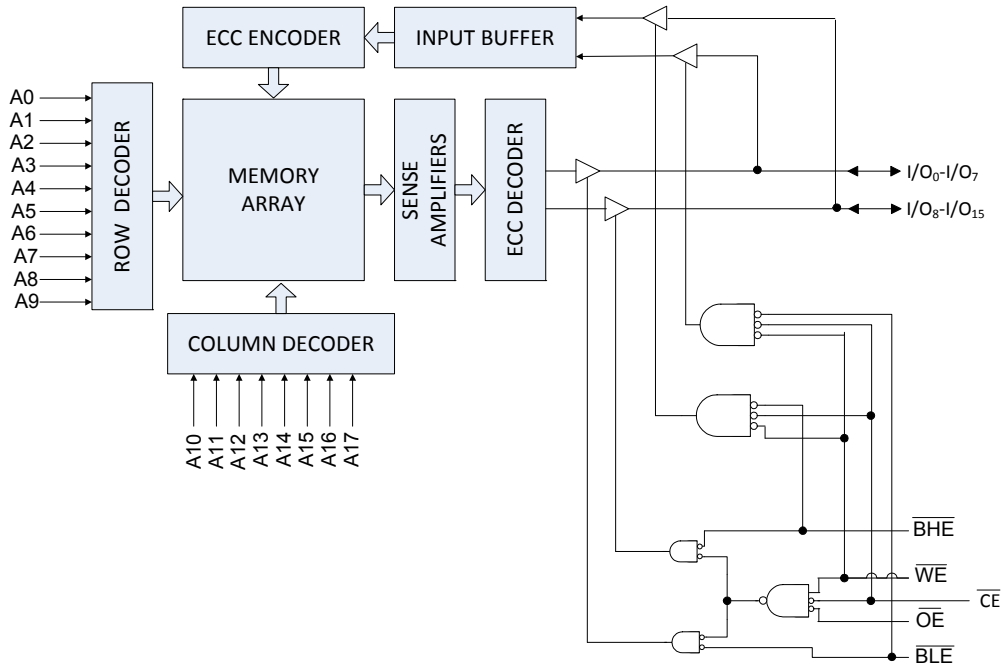
The device also has a unique Byte Power down feature, where, if both the Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enables, thereby saving power.

The logic block diagrams are on page 2.

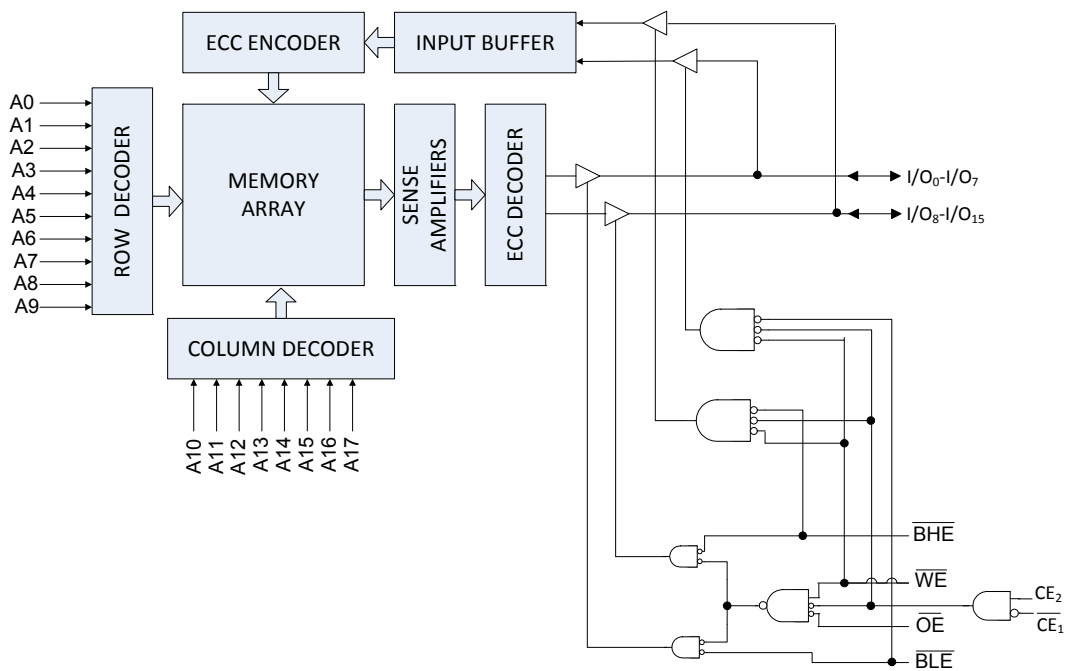
#### Note

1. This device does not support automatic write-back on error detection.

**Logic Block Diagram – CY62147G**



**Logic Block Diagram – CY621472G**



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### Pin Configuration – CY62147G

Figure 1. 48-ball VFPGA pinout (Single Chip Enable without ERR) – CY62147G [2]

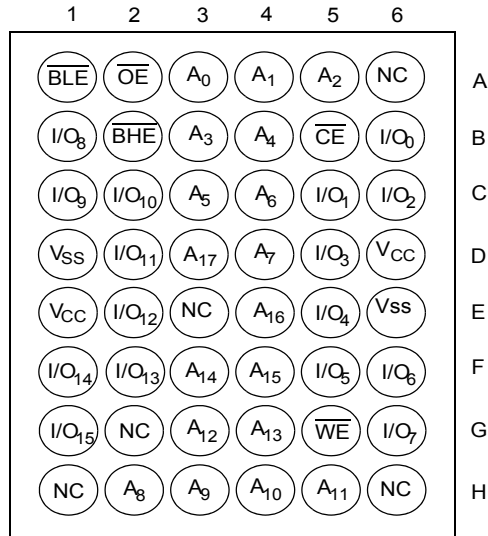
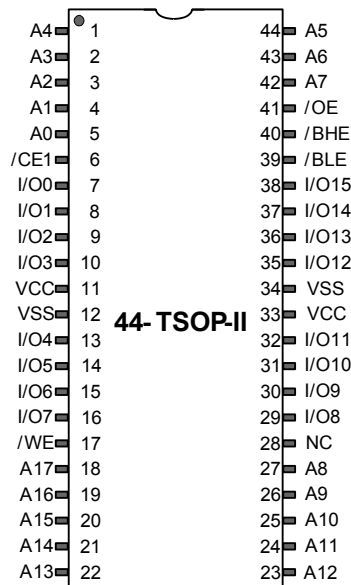


Figure 2. 44-pin TSOP II pinout (Single Chip Enable without ERR) – CY62147G [2]

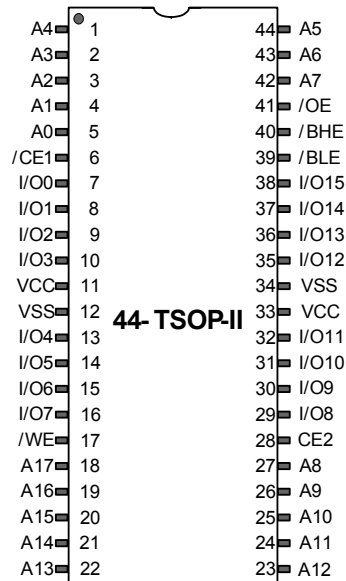


**Note**

2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

## Pin Configuration – CY621472G

Figure 3. 44-pin TSOP II pinout (Dual Chip Enable without ERR) – CY621472G



## Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation			
					Operating I <sub>CC</sub> , (mA)		Standby, I <sub>SB2</sub> (μA)	
					f = f <sub>max</sub>			
					Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62147G30/ CY621472G30	Single or dual Chip Enables	Automotive-A	2.2 V–3.6 V	45	15	20	3.5	8.7
		Automotive-E		55	15	24	–	35

**Note**

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature  
with power applied ..... -55 °C to + 125 °C

Supply voltage  
to ground potential <sup>[4]</sup> ..... -0.3 V to V<sub>CC</sub> + 0.3 V

DC voltage applied to outputs  
in HI-Z state <sup>[4]</sup> ..... -0.3 V to V<sub>CC</sub> + 0.3 V

DC input voltage <sup>[4]</sup> ..... -0.3 V to V<sub>CC</sub> + 0.3 V

Output current into outputs (in low state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

## Operating Range

Grade	Ambient Temperature	V <sub>CC</sub>
Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V
Automotive-E	-40 °C to +125 °C	

## DC Electrical Characteristics

Over the operating range

Parameter	Description		Test Conditions	45 ns (Automotive-A)			55 ns (Automotive-E)			Unit	
				Min	Typ	Max	Min	Typ	Max		
V <sub>OH</sub>	Output HIGH voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	2	-	-	2	-	-	V	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.4	-	-	2.4	-	-		
V <sub>OL</sub>	Output LOW voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.4	-	-	0.4	V	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	-	-	0.4	-	-	0.4		
V <sub>IH</sub>	Input HIGH voltage	2.2 V to 2.7 V	-	1.8	-	V <sub>CC</sub> + 0.3 <sup>[4]</sup>	2	-	V <sub>CC</sub> + 0.3 <sup>[4]</sup>	V	
		2.7 V to 3.6 V	-	2	-	V <sub>CC</sub> + 0.3 <sup>[4]</sup>	2	-	V <sub>CC</sub> + 0.3 <sup>[4]</sup>		
V <sub>IL</sub>	Input LOW voltage	2.2 V to 2.7 V	-	-0.3 <sup>[4]</sup>	-	0.6	-0.3 <sup>[4]</sup>	-	0.6	V	
		2.7 V to 3.6 V	-	-0.3 <sup>[4]</sup>	-	0.8	-0.3 <sup>[4]</sup>	-	0.8		
I <sub>Ix</sub>	Input leakage current		GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	-5	-	+5	μA	
I <sub>OZ</sub>	Output leakage current		GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	-	+1	-5	-	+5	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current		Max V <sub>CC</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	f = f <sub>MAX</sub>	-	15	20	-	15	24	mA
				f = 1 MHz	-	3.5	6	-	3.5	10	

### Note

4. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.

**DC Electrical Characteristics** (continued)

Over the operating range

Parameter	Description	Test Conditions	45 ns (Automotive-A)			55 ns (Automotive-E)			Unit
			Min	Typ	Max	Min	Typ	Max	
$I_{SB1}^{[5]}$	Automatic power down current – CMOS inputs; $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , $f = f_{max}$ (address and data only), $f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), Max $V_{CC}$	–	3.5	8.7	–	–	35	$\mu\text{A}$
$I_{SB2}^{[5]}$	Automatic power down current – CMOS inputs $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , $f = 0$ , Max $V_{CC}$	–	3.5	8.7	–	–	35	$\mu\text{A}$

**Note**

5. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

### Capacitance

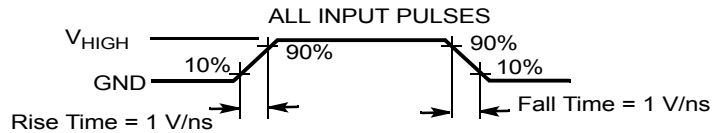
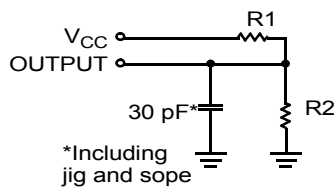
Parameter [6]	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

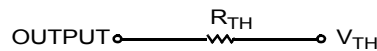
Parameter [6]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.17	66.82	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		14.90	15.97	°C/W

### AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [7]



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R <sub>1</sub>	13500	16667	1103	1800	Ω
R <sub>2</sub>	10800	15385	1554	990	Ω
R <sub>TH</sub>	6000	8000	645	639	Ω
V <sub>TH</sub>	0.80	1.20	1.75	1.77	V

**Notes**

- 6. Tested initially and after any design or process changes that may affect these parameters.
- 7. Full-device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.



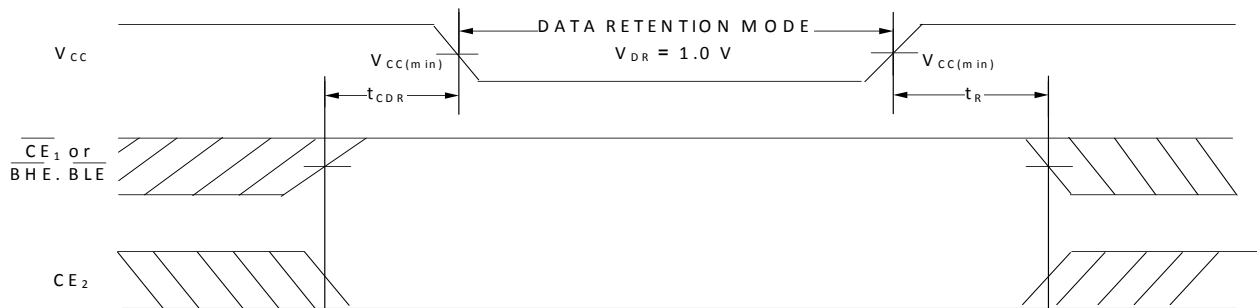
## Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	(Automotive-A)			(Automotive-E)			Unit
			Min	Typ <sup>[8]</sup>	Max	Min	Typ <sup>[8]</sup>	Max	
$V_{DR}$	$V_{CC}$ for data retention		1	–	–	1	–	–	V
$I_{CCDR}^{[9, 10]}$	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	13	–	–	50	$\mu\text{A}$
$t_{CDR}^{[11]}$	Chip deselect to data retention time		0	–	–	0	–	–	ns
$t_R^{[11, 12]}$	Operation recovery time		45	–	–	55	–	–	ns

## Data Retention Waveform

Figure 5. Data Retention Waveform <sup>[13]</sup>



### Notes

- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8\text{ V}$  (for  $V_{CC}$  range of  $1.65\text{ V}$ – $2.2\text{ V}$ ),  $V_{CC} = 3\text{ V}$  (for  $V_{CC}$  range of  $2.2\text{ V}$ – $3.6\text{ V}$ ), and  $V_{CC} = 5\text{ V}$  (for  $V_{CC}$  range of  $4.5\text{ V}$ – $5.5\text{ V}$ ),  $T_A = 25\text{ }^\circ\text{C}$ .
- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
- $I_{CCDR}$  is guaranteed only after the device is first powered up to  $V_{CC(\text{min})}$  and then brought down to  $V_{DR}$ .
- These parameters are guaranteed by design.
- Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ .
- $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## AC Switching Characteristics

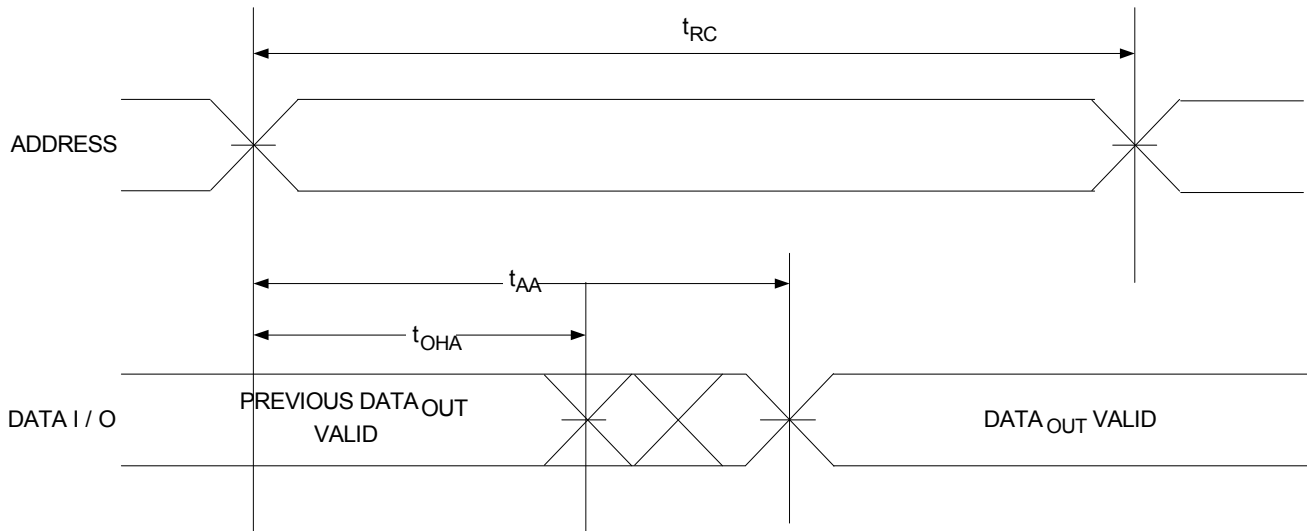
Parameter <sup>[14]</sup>	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	45	–	55	–	ns
$t_{AA}$	Address to data valid	–	45	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	10	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid	–	45	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low impedance <sup>[15, 16]</sup>	5	–	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to HI-Z <sup>[15, 16, 17]</sup>	–	18	–	18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low impedance <sup>[15, 16]</sup>	10	–	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to HI-Z <sup>[15, 16, 17]</sup>	–	18	–	18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up <sup>[16]</sup>	0	–	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to power-down <sup>[16]</sup>	–	45	–	55	ns
$t_{DBE}$	$\overline{BLE} / \overline{BHE}$ LOW to data valid	–	45	–	55	ns
$t_{LZBE}$	$\overline{BLE} / \overline{BHE}$ LOW to Low impedance <sup>[15, 16]</sup>	5	–	5	–	ns
$t_{HZBE}$	$\overline{BLE} / \overline{BHE}$ HIGH to HI-Z <sup>[15, 16, 17]</sup>	–	18	–	18	ns
<b>Write Cycle</b> <sup>[18, 19]</sup>						
$t_{WC}$	Write cycle time	45	–	55	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	35	–	40	–	ns
$t_{AW}$	Address setup to write end	35	–	40	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	40	–	ns
$t_{BW}$	$\overline{BLE} / \overline{BHE}$ LOW to write end	35	–	45	–	ns
$t_{SD}$	Data setup to write end	25	–	25	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to HI-Z <sup>[15, 16, 17]</sup>	–	18	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low impedance <sup>[15, 16]</sup>	10	–	10	–	ns

### Notes

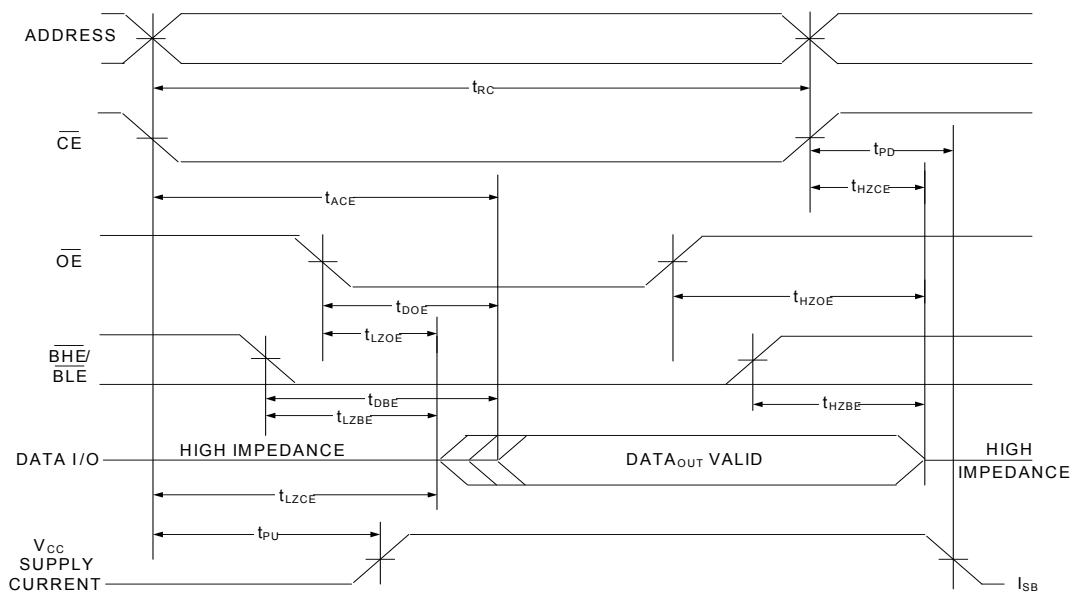
14. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
15. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
16. These parameters are guaranteed by design.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
19. The minimum pulse width in Write Cycle No 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 6. Read Cycle No. 1 of CY62147G/CY621472G (Address Transition Controlled)** [20, 21]



**Figure 7. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [21, 22, 23]

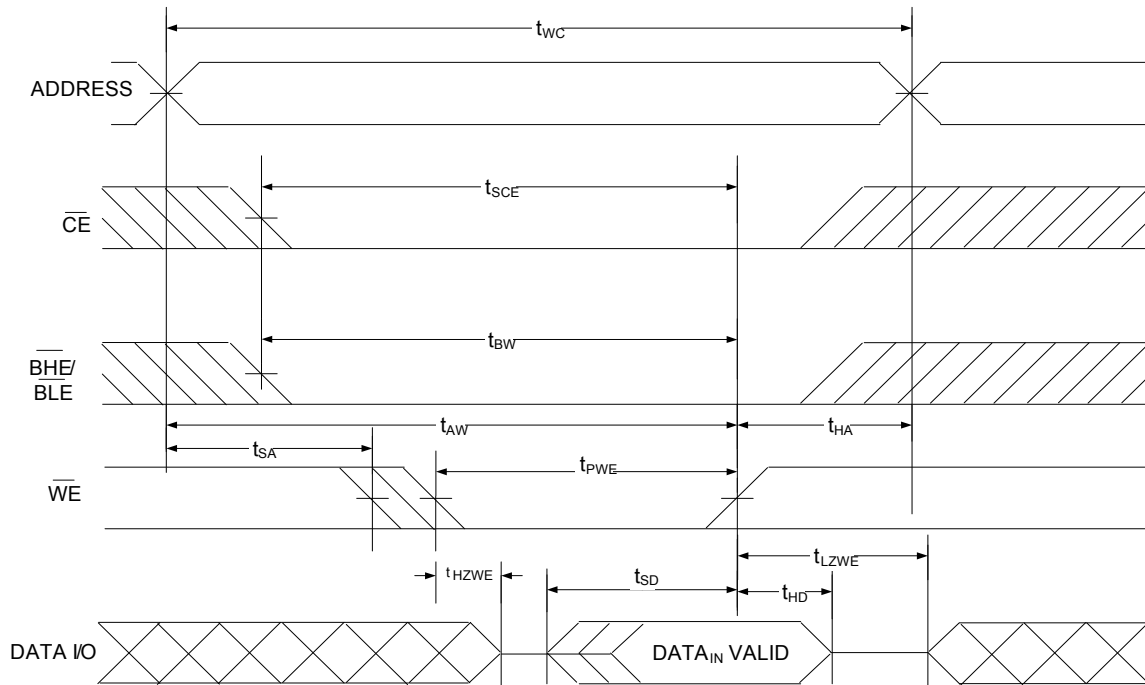


### Notes

20. The device is continuously selected.  $\overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ .
21.  $\overline{\text{WE}}$  is HIGH for Read cycle.
22. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
23. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.

**Switching Waveforms** (continued)

**Figure 8. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [24, 25, 26]

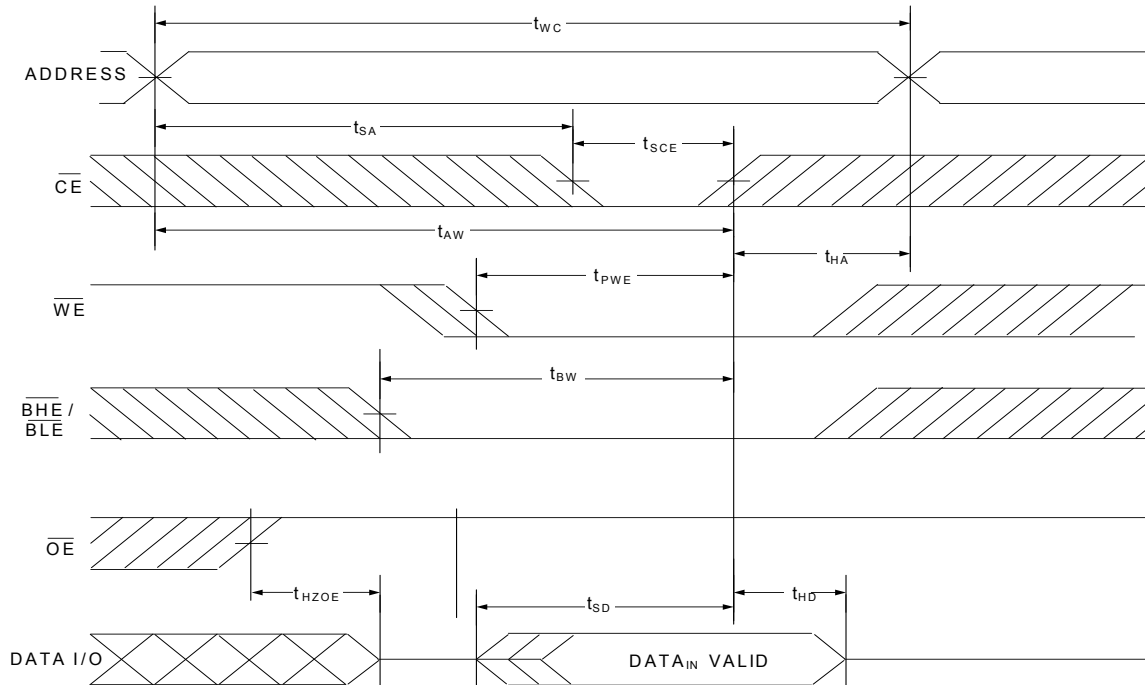


**Notes**

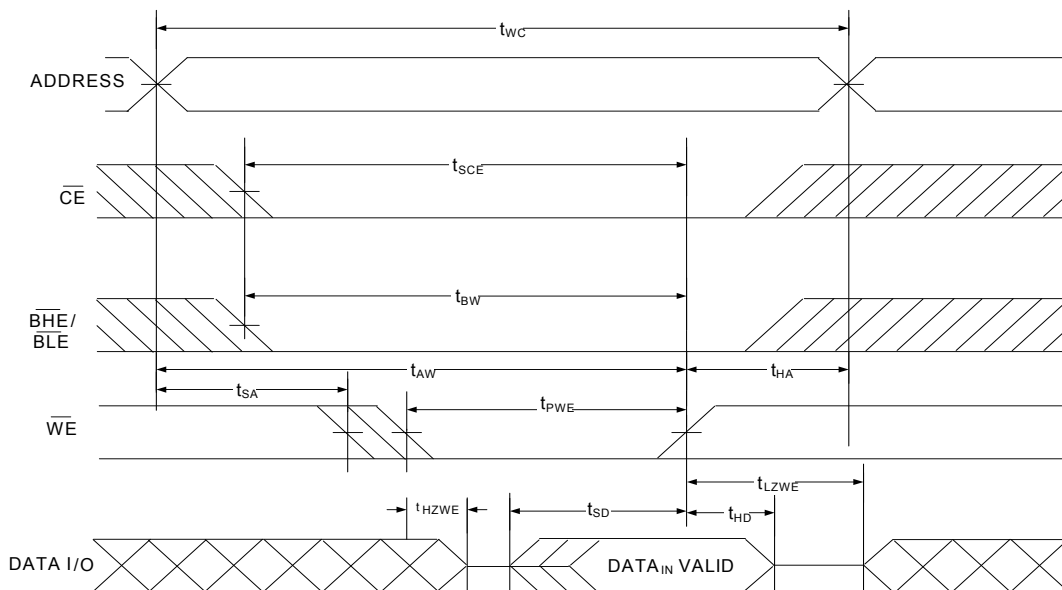
- 24. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
- 25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 26. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

**Switching Waveforms** (continued)

**Figure 9. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [27, 28, 29]



**Figure 10. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [27, 28, 29, 30]

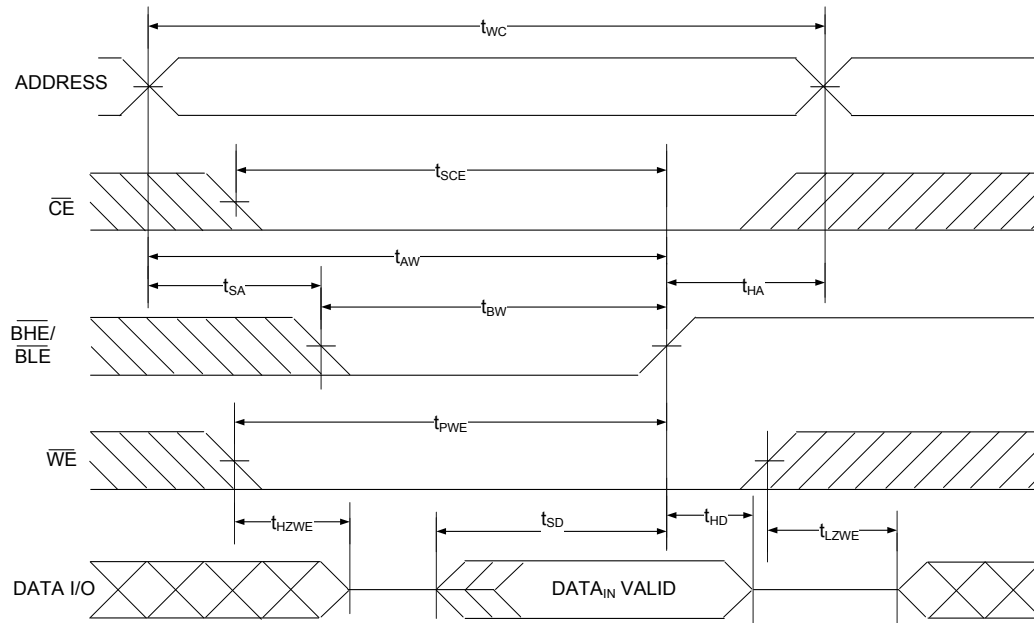


**Notes**

27. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
28. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
30. The minimum write pulse width for Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

Switching Waveforms (continued)

Figure 11. Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled) [31, 32, 33]



Notes

31. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
32. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
33. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

**Truth Table – CY62147G/CY621472G**

$\overline{CE} / \overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X <sup>[34]</sup>	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X <sup>[34]</sup>	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X <sup>[34]</sup>	X <sup>[34]</sup>	X	X	H	H	HI-Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	H	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); HI-Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	L	L	H	HI-Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	H	L	H	HI-Z	Output disabled	Active (I <sub>CC</sub> )
L	H	H	H	H	L	HI-Z	Output disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	L	HI-Z	Output disabled	Active (I <sub>CC</sub> )
L	H	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	H	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); HI-Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	H	L	X	L	H	HI-Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data In (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )

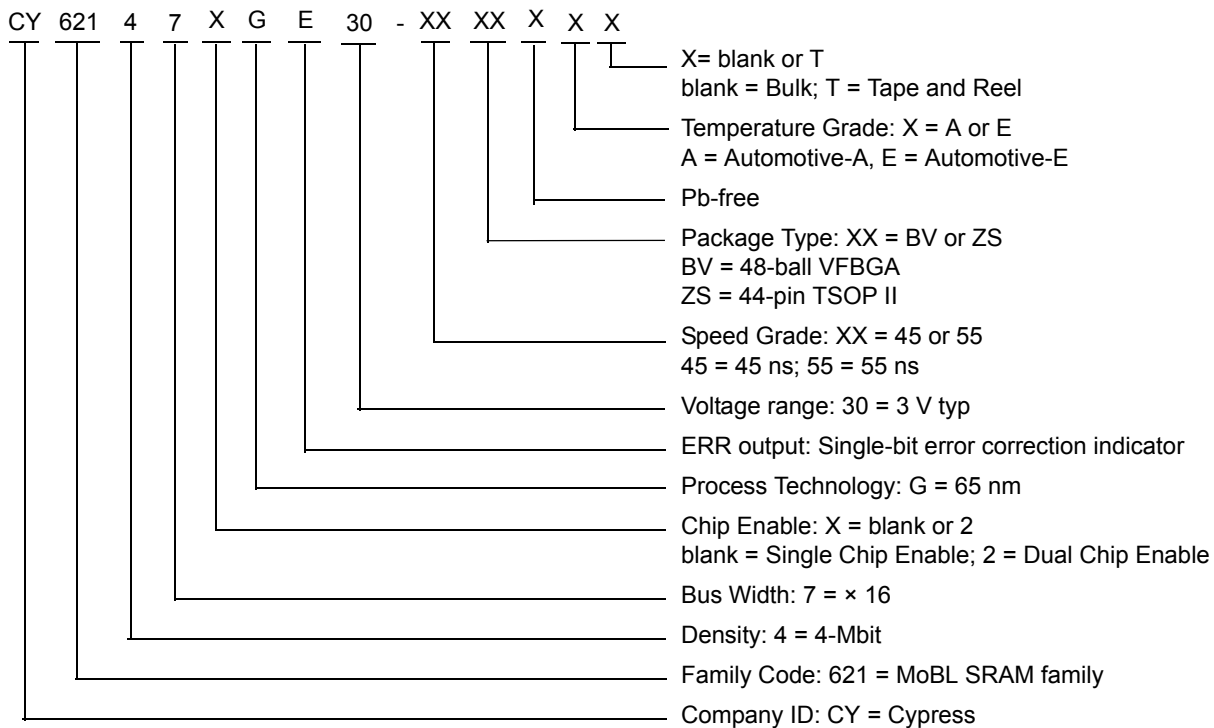
**Note**

34. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

**Ordering Information**

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62147G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	Automotive-A
		CY62147G30-45BVXAT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY62147G30-45ZSXA	51-85087	44-pin TSOP II without ERR	
		CY62147G30-45ZSXAT	51-85087	44-pin TSOP II without ERR, Tape and Reel	
		CY621472G30-45ZSXA	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY621472G30-45ZSXAT	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
55	2.2 V–3.6 V	CY62147G30-55BVXE	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	Automotive-E
		CY62147G30-55BVXET	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY62147G230-55ZSXE	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY62147G230-55ZSXET	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
		CY62147G30-55ZSXE	51-85087	44-pin TSOP II	
		CY62147G30-55ZSXET	51-85087	44-pin TSOP II, Tape and Reel	

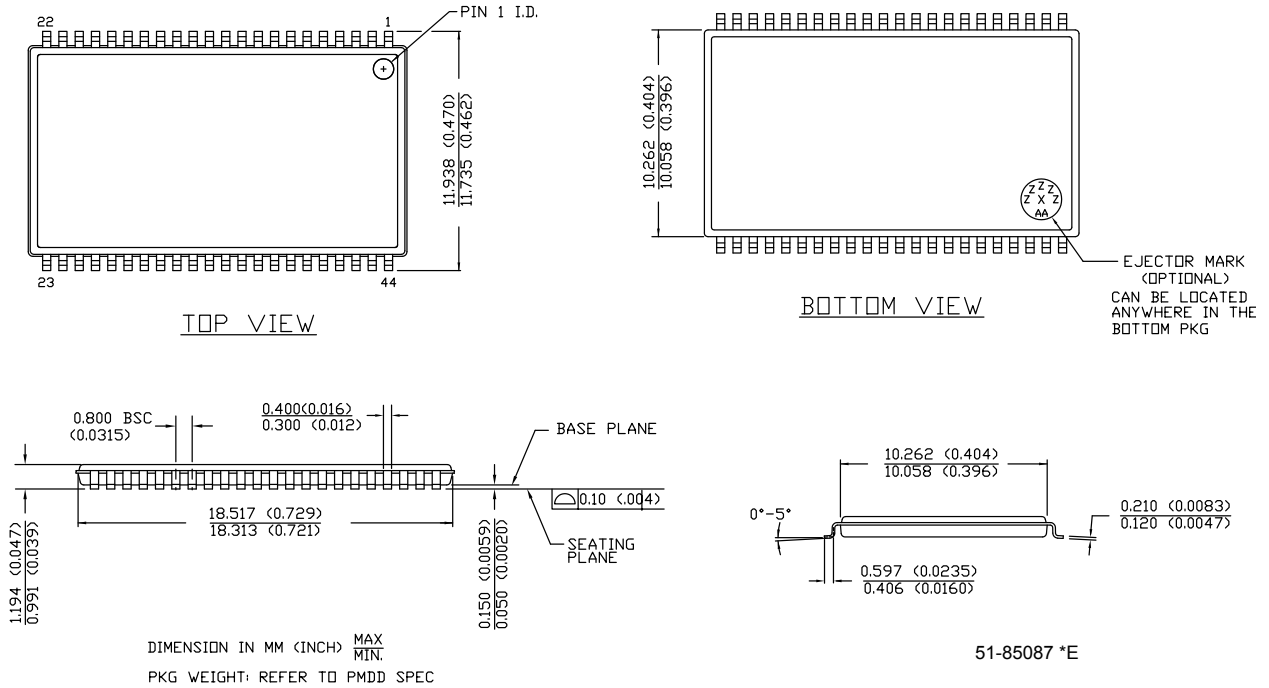
**Ordering Code Definitions**



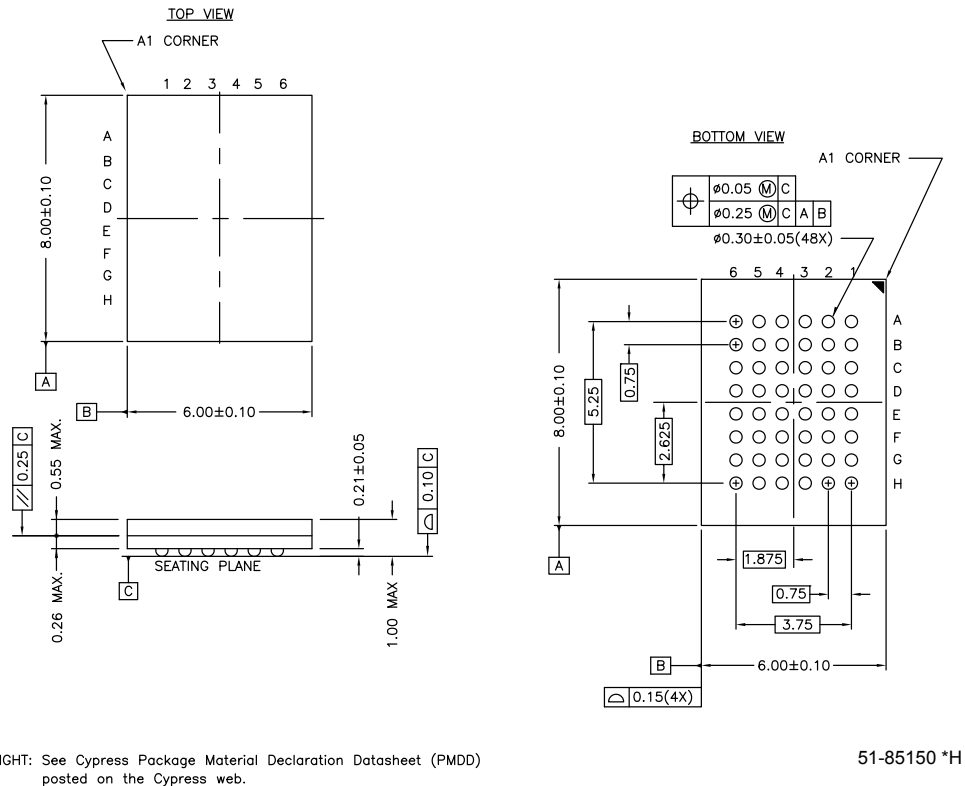


**Package Diagrams**

**Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087**



**Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62147G/CY621472G MoBL® Automotive, 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)				
Document Number: 001-95424				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5032662	NILE	12/01/2015	Changed status from Preliminary to Final.
*C	5428830	NILE	09/07/2016	<p>Updated <a href="#">Maximum Ratings</a>: Updated Note 4 (Replaced “2 ns” with “20 ns”).</p> <p>Updated <a href="#">DC Electrical Characteristics</a>: Changed minimum value of <math>V_{OH}</math> parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “<math>V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}</math>”.</p> <p>Changed minimum value of <math>V_{IH}</math> parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”.</p> <p>Updated <a href="#">Ordering Information</a>: Updated part numbers. Updated to new template.</p>

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