19-5657; Rev 1; 1/11

MAXIM

Gigabit Multimedia Deserializer with Spread Spectrum and Full-Duplex Control Channel

General Description

The MAX9270 deserializer uses Maxim's gigabit multimedia serial link (GMSL) technology. The device functions the same as the MAX9260 deserializer without an output enable ($\overline{ENABLE}$) pin. Outputs are enabled or disabled by a register bit. The deserializer pairs with any GMSL serializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data.

The deserializer accepts a maximum serial payload data rate of 2.5Gbps for a 15m shielded twisted-pair (STP) cable. The 24-bit or 32-bit width parallel interface operates up to a maximum bus clock of 104MHz or 78MHz, respectively. This serial link supports display panels from QVGA (320 x 240) up to XGA (1280 x 768), or dual-view WVGA (2 x 854 x 480).

The 24-bit or 32-bit mode handles 21 or 29 bits of data, along with an I²S input, supporting 4- to 32-bit audio word lengths and an 8kHz to 192kHz sample rate. The embedded control channel forms a full-duplex, differential 100kbps to 1Mbps UART link between the serializer and deserializer. The host electronic control unit (ECU) or microcontroller (µC) resides either on the serializer (for video display) or the deserializer (for image sensing). In addition, the control channel enables ECU/µC control of peripherals in the remote side of the serial link through I²C (base mode) or a user-defined full-duplex UART format (bypass mode).

The channel equalizer extends the link length and enhances the link reliability. Spread spectrum is available to reduce EMI on the parallel output data signals. The differential link complies with the ISO 10605 and IEC 61000-4-2 ESD-protection standards.

This device uses a 3.3V core supply and a 1.8V to 3.3V I/O supply. The device is available in a 56-pin TQFN package (8mm x 8mm x 0.75mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +105°C automotive temperature range.

Applications

High-Speed Serial-Data Transmission for Display

High-Speed Serial-Data Transmission for Image Sensing

Automotive Navigation, Infotainment, and Image-Sensing Systems

Features

- **Pairs with Any GMSL Serializer**
- **2.5Gbps Payload Rate, AC-Coupled Serial Link with 8b/10b Line Coding**
- **24-Bit or 32-Bit Programmable Parallel Output Bus Supports Up to XGA (1280 x 768) or Dual-View WVGA (2 x 854 x 480) Panels with 18-Bit or 24-Bit Color**
- **8.33MHz to 104MHz (24-Bit Bus) or 6.25MHz to 78MHz (32-Bit Bus) Parallel Data Rate**
- **Support Two/Three 10-Bit Camera Links at 104MHz/78MHz Maximum Pixel Clock**
- **4-Bit to 32-Bit Word Length, 8kHz to 192kHz I²S Audio Channel Supports High-Definition Audio**
- **Embedded Half-/Full-Duplex Bidirectional Control Channel (100kbps to 1Mbps)**
- **Separate Interrupt Signal Supports Touch-Screen Functions for Display Panels**
- **Remote-End I²C Master for Peripherals**
- **Line Equalizer Extends Link Length**
- **Programmable Spread Spectrum on the Parallel Data Outputs Reduce EMI**
- **Does Not Require an External Clock**
- **Auto Data-Rate Detection Allows "On-The-Fly" Data-Rate Change**
- **Built-In PRBS Checker for BER Testing**
- **ISO 10605 and IEC 61000-4-2 ESD Protection**
- **-40°C to +105°C Operating Temperature Range**
- **Patent Pending**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9270GTN/V+	-40°C to +105°C	56 TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Typical Applications Circuit appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

AVDD to EP ..... -0.5V to +3.9V
DVDD to EP ..... -0.5V to +3.9V
IOVDD to EP ..... -0.5V to +3.9V
IN+, IN- to EP ..... -0.5V to +1.9V
All Other Pins to EP ..... -0.5V to (IOVDD + 0.5V)
IN+, IN- Short Circuit to Ground or Supply ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
(IN+, IN-) to EP ..... ±8kV
All Other Pins to EP ..... ±4kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge
(IN+, IN-) to EP ..... ±8kV
Air Discharge
(IN+, IN-) to EP ..... ±10kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge
(IN+, IN-) to EP ..... ±8kV
Air Discharge
(IN+, IN-) to EP ..... ±20kV
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

56 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (ENABLE, INT, PWDN, SSEN, BWS, ES, DRS, MS, CDS, EQS, DCS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUTS (DOUT_, SD, WS, SCK, PCLKOUT)							
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA	V_{DCS} = V_{GND}	V_{IOVDD} - 0.3			V
			V_{DCS} = V_{IOVDD}	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA	V_{DCS} = V_{GND}			0.3	V
			V_{DCS} = V_{IOVDD}			0.2	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	DOUT_, SD, WS, SCK	V_O = 0V, V_{DCS} = V_{GND}	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, V_{DCS} = V_{GND}	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{ERR}$, GPIO_, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)	RX/SDA, TX/SCL		-110		+1	µA
			GPIO, $\overline{ERR}$, LOCK		-80		+1	
Low-Level Open-Drain Output Voltage	V_{OL2}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V				0.4	V
			V_{IOVDD} = 3.0V to 3.6V				0.3	V
DIFFERENTIAL OUTPUTS FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROH}	No high-speed data transmission (Figure 1)			30		60	mV
Differential Low Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROL}	No high-speed data transmission (Figure 1)			-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)								
Differential High Input Threshold (Peak), (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	(Figure 2)				40	90	mV
Differential Low Input Threshold (Peak), (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	(Figure 2)			-90	-40		mV
Input Common-Mode Voltage, ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}				1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I				80	100	130	Ω

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Worst-Case Supply Current (Figure 3)	I_{WCS}	V_{BWS} = V_{GND}, $f_{PCLKOUT}$ = 16.6MHz	2% spread spectrum active		113	166	mA
			Spread spectrum disabled		105	155	
		V_{BWS} = V_{GND}, $f_{PCLKOUT}$ = 33.3MHz	2% spread spectrum active		122	181	
			Spread spectrum disabled		110	165	
		V_{BWS} = V_{GND}, $f_{PCLKOUT}$ = 66.6MHz	2% spread spectrum active		137	211	
			Spread spectrum disabled		120	188	
		V_{BWS} = V_{GND}, $f_{PCLKOUT}$ = 104MHz	2% spread spectrum active		159	247	
			Spread spectrum disabled		135	214	
Sleep-Mode Supply Current	I_{CCS}				80	130	µA
Power-Down Supply Current	I_{CCZ}	$V_{\overline{PWDN}}$ = V_{GND}			19	70	µA

AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)						
Clock Frequency	$f_{PCLKOUT}$	V_{BWS} = V_{GND}, V_{DRS} = V_{IOVDD}	8.33		16.66	MHz
		V_{BWS} = V_{GND}, V_{DRS} = V_{GND}	16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}	6.25		12.5	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{GND}	12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 4)	40	50	60	%
Clock Jitter	t_J	Period jitter, RMS, spread off, 3.125Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$		0.05		UI
I²C/UART PORT TIMING						
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 5)	100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 5)	0			ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS							
PCLKOUT Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.4		2.2	ns
			V_{DCS} = V_{GND}, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.25		1.7	
			V_{DCS} = V_{GND}, C_L = 5pF	0.3		2.0	
Parallel Data Rise-and-Fall Time (Figure 6)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.5		3.1	ns
			V_{DCS} = V_{GND}, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		2.2	
			V_{DCS} = V_{GND}, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	Spread spectrum enabled (Figure 7)				2880	Bits
		Spread spectrum disabled (Figure 7)				750	
Lock Time	t_{LOCK}	Spread spectrum enabled (Figure 8)				1500	µs
		Spread spectrum off (Figure 8)				1000	
Power-Up Time	t_{PU}	(Figure 9)				2500	µs
Reverse Control-Channel Output Rise Time	t_R	No high-speed transmission (Figure 1)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No high-speed transmission (Figure 1)		180		400	ns
I²S OUTPUT TIMING							
WS Jitter	t_{AJ-WS}	t_{WS} = 1/f_{WS}, rising (falling) edge to falling (rising) edge (Note 3)	f_{WS} = 48kHz or 44.1kHz		0.4e - 3 x t_{WS}	0.5e - 3 x t_{WS}	ns
			f_{WS} = 96kHz		0.8e - 3 x t_{WS}	1e - 3 x t_{WS}	
			f_{WS} = 192kHz		1.6e - 3 x t_{WS}	2e - 3 x t_{WS}	
SCK Jitter	t_{AJ-SCK}	t_{SCK} = 1/f_{SCK}, rising edge to rising edge	n_{WS} = 16 bits, f_{WS} = 48kHz or 44.1kHz		13e - 3 x t_{SCK}	16e - 3 x t_{SCK}	ns
			n_{WS} = 24 bits, f_{WS} = 96kHz		39e - 3 x t_{SCK}	48e - 3 x t_{SCK}	
			n_{WS} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

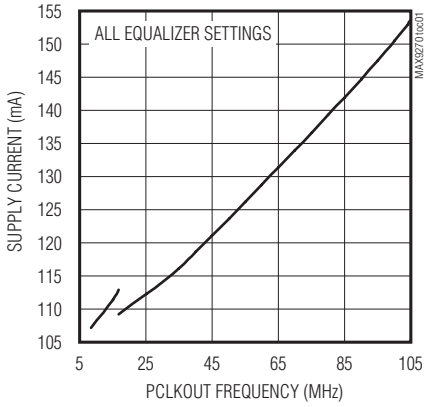
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Audio Skew Relative to Video	ASK	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		3.1	ns
			V_{DCS} = V_{GND}, C_L = 5pF	0.4		3.8	ns
SD, WS Valid Time Before SCK	t_{DVB}	t_{SCK} = 1/f_{SCK} (Figure 11)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{DVA}	t_{SCK} = 1/f_{SCK} (Figure 11)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.
Note 3: Rising to rising edge jitter can be twice as large.

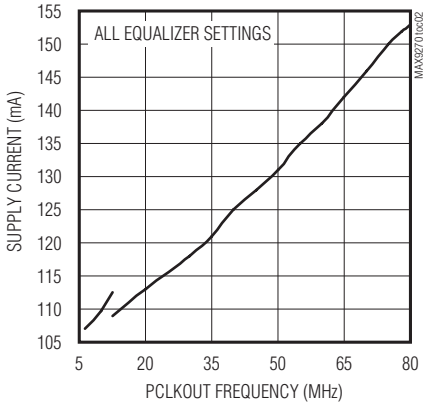
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

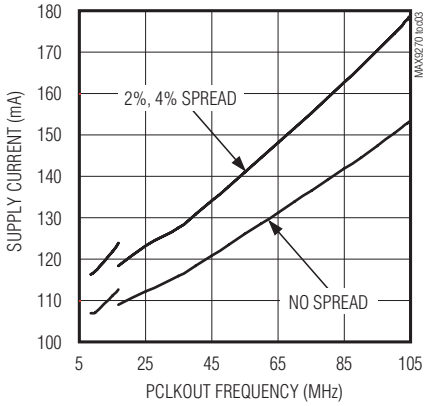
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (24-BIT MODE)



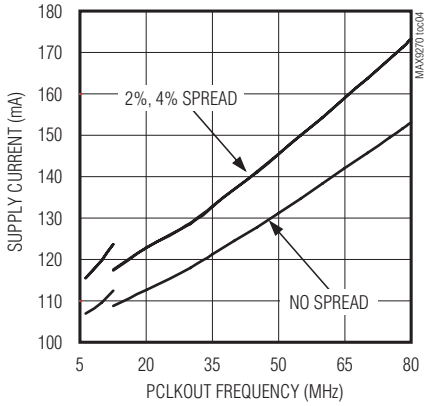
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (32-BIT MODE)



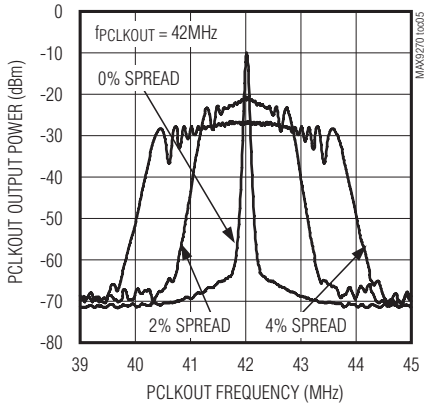
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (24-BIT MODE)



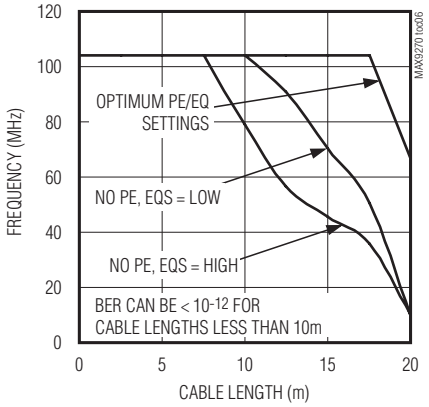
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (32-BIT MODE)



OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY



MAXIMUM PCLKIN FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-9})



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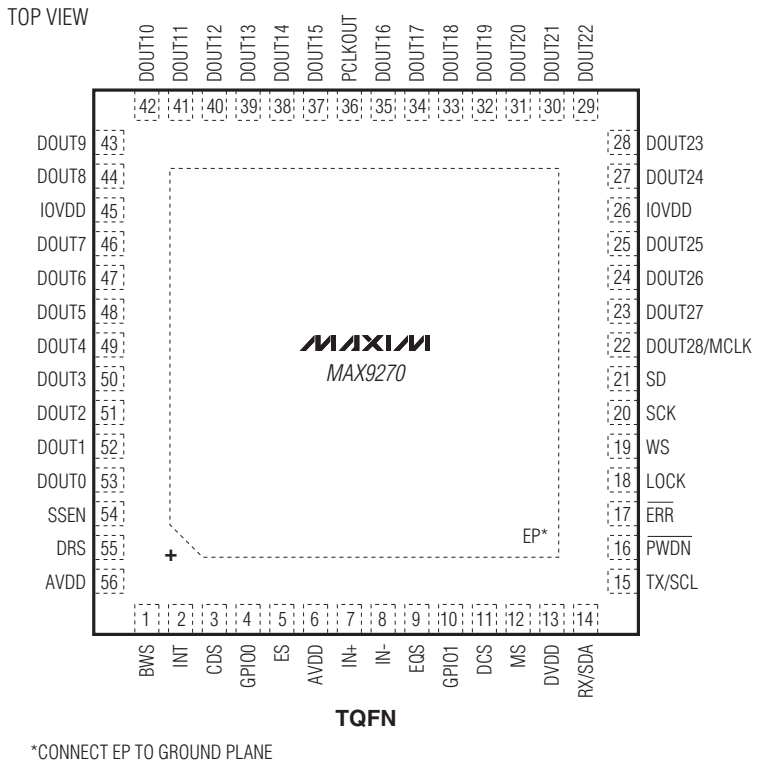
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	BWS	Bus-Width Select. Parallel output bus-width selection input requires external pulldown or pullup resistors. Set BWS = low for 24-bit bus mode. Set BWS = high for 32-bit bus mode.
2	INT	Interrupt. Interrupt input requires external pulldown or pullup resistors. A transition on the INT input of the deserializer toggles the serializer's INT output.
3	CDS	Control-Direction Selection. Control-link-direction selection input requires external pull-down or pullup resistors. Set CDS = low for µC use on the serializer side of the serial link. Set CDS = high for µC use on the deserializer side of the serial link.
4	GPIO0	GPIO0. Open-drain general-purpose input/output with internal 60kΩ pullup resistors to IOVDD. GPIO0 is high impedance during power-up and when $\overline{PWDN}$ = low.
5	ES	Edge Select. PCLKOUT edge-selection input requires external pulldown or pullup resistors. Set ES = low for a rising-edge trigger. Set ES = high for a falling-edge trigger.

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Pin Description (continued)

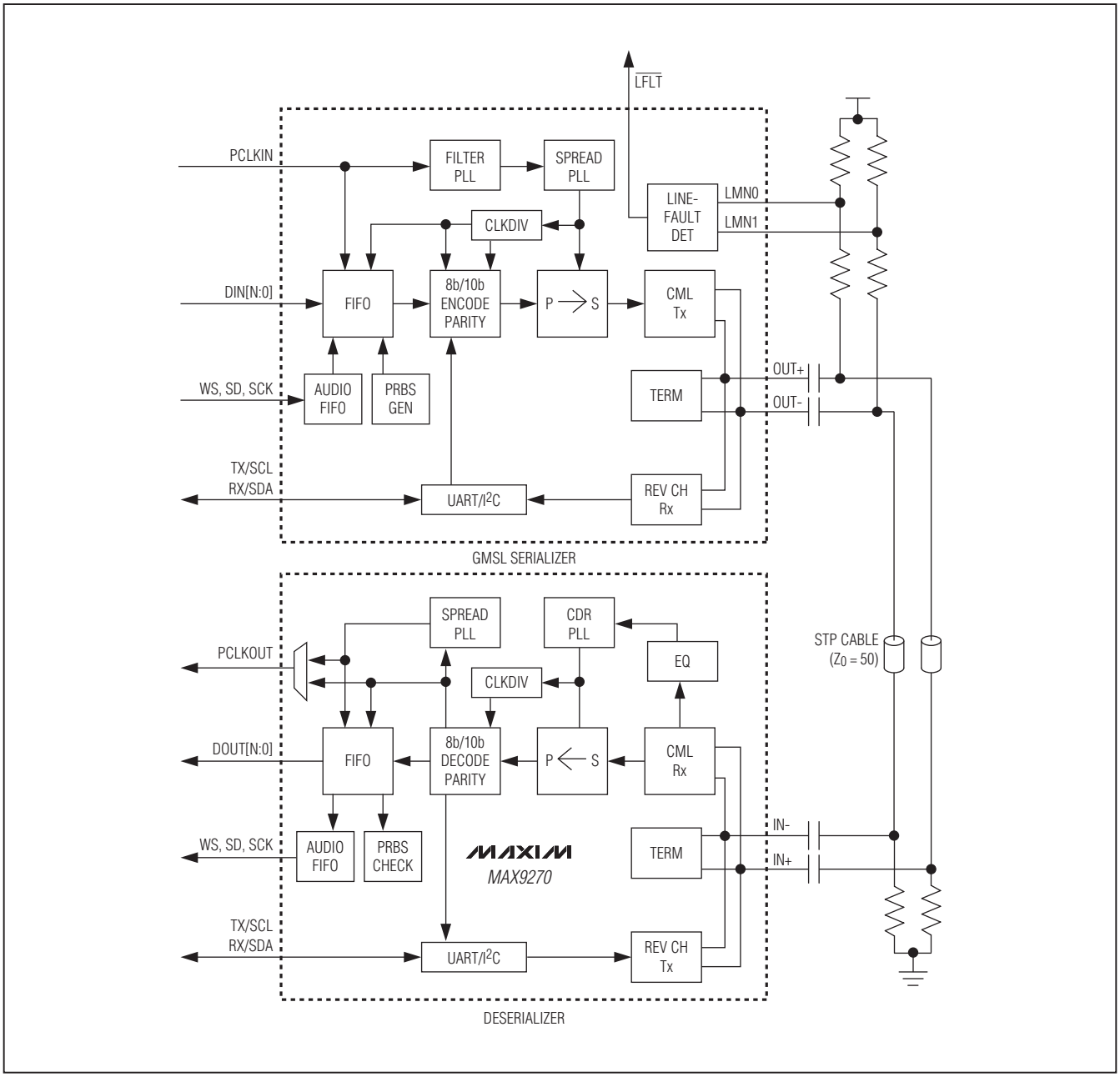
PIN	NAME	FUNCTION
6, 56	AVDD	3.3V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to AVDD.
7, 8	IN+, IN-	Differential CML Input +/−. Differential inputs of the serial link.
9	EQS	Equalizer Select. Deserializer equalizer-selection input requires external pulldown or pullup resistors. The state of EQS latches upon power-up or rising edge of $\overline{PWDN}$. Set EQS = low for 10.7dB equalizer boost (EQTUNE = 1001). Set EQS = high for 5.2dB equalizer boost (EQTUNE = 0100).
10	GPIO1	GPIO1. Open-drain general-purpose input/output with internal 60kΩ pullup resistors to IOVDD. GPIO1 is high impedance during power-up and when $\overline{PWDN}$ = low.
11	DCS	Drive Current Select. Driver current-selection input requires external pulldown or pullup resistors. Set DCS = high for stronger parallel data and clock output drivers. Set DCS = low for normal parallel data and clock drivers (see the *DC Electrical Characteristics* table).
12	MS	Mode Select. Control-link mode-selection/autostart mode selection input requires external pulldown or pullup resistors. MS sets the control-link mode when CDS = high (see the *Control-Channel and Register Programming* section). Set MS = low to select base mode. Set MS = high to select the bypass mode. MS sets autostart mode when CDS = low (see Tables 13 and 14).
13	DVDD	3.3V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
14	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the deserializer's UART. In I²C mode, RX/SDA is the SDA input/output of the serializer's I²C master.
15	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In I²C mode, TX/SCL is the SCL output of the deserializer's I²C master.
16	$\overline{PWDN}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistors.
17	$\overline{ERR}$	Error. Active-low open-drain video data error output with internal pullup to IOVDD. $\overline{ERR}$ goes low when the number of decoding errors during normal operation exceed a programmed error threshold or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ is high impendence when $\overline{PWDN}$ = low.
18	LOCK	Open-Drain Lock Output with Internal Pullup to IOVDD. LOCK = high indicates PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates PLLs are not locked or incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active. LOCK is high impedance when $\overline{PWDN}$ = low.
19	WS	Word Select. I²S word-select output.
20	SCK	Serial Clock. I²S serial-clock output
21	SD	Serial Data. I²S serial-data output. Disable I²S to use SD as an additional data output latched on the selected edge of PCLKOUT.

Pin Description (continued)

PIN	NAME	FUNCTION
22–25, 27–35, 37–44, 46–53	DOUT28/MCLK, DOUT27, DOUT26, DOUT25, DOUT24–DOUT16, DOUT15–DOUT8, DOUT7–DOUT0	Data Output[0:28]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. Set BWS = low (24-bit mode) to use DOUT0–DOUT20 (RGB and SYNC). DOUT21–DOUT28 are not used in 24-bit mode and are set to low. Set BWS = high (32-bit mode) to use DOUT0–DOUT28 (RGB, SYNC, and two extra outputs). DOUT28 can be used to output MCLK (see the *Additional MCLK Output for Audio Applications* section).
26, 45	IOVDD	1.8V to 3.3V Logic I/O Power Supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to IOVDD.
36	PCLKOUT	Parallel Clock Output. Used for DOUT0–DOUT28.
54	SSEN	Spread-Spectrum Enable. Parallel output spread-spectrum enable input requires external pulldown or pullup resistors. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±2% spread spectrum on the parallel outputs. Set SSEN = low to use the parallel outputs without spread spectrum.
55	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistors. Set DRS = high for parallel input data rates of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for parallel input data rates of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
—	EP	Exposed Pad. EP functions as the IC's ground connection. **MUST** connect EP to the ground plane to maximize thermal and electrical performance.

Gigabit Multimedia Deserializer with Spread Spectrum and Full-Duplex Control Channel

Functional Diagram



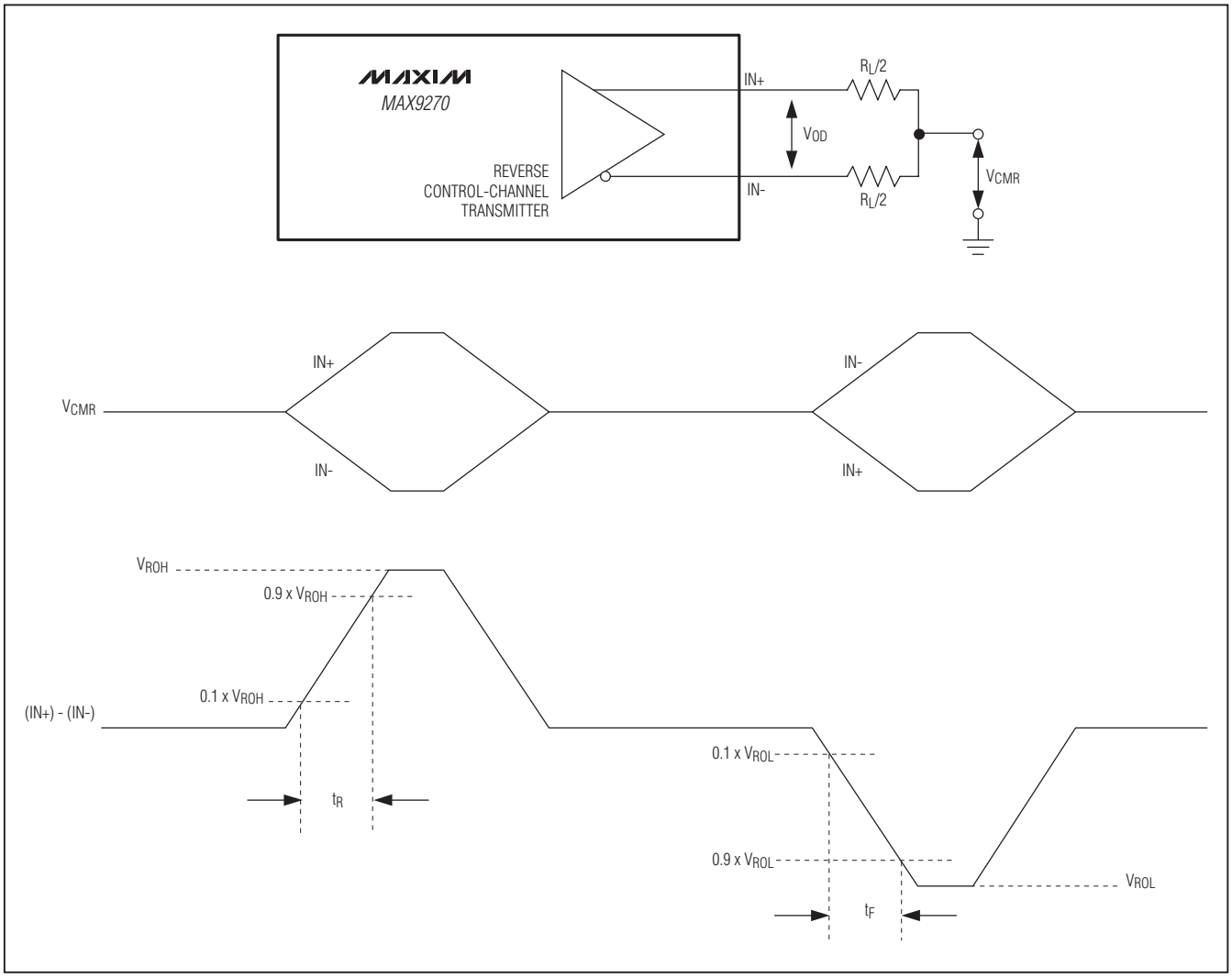


Figure 1. Reverse Control-Channel Output Parameters

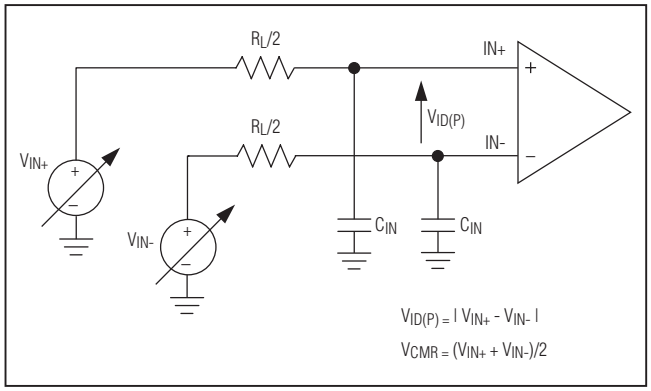


Figure 2. Test Circuit for Differential Input Measurement

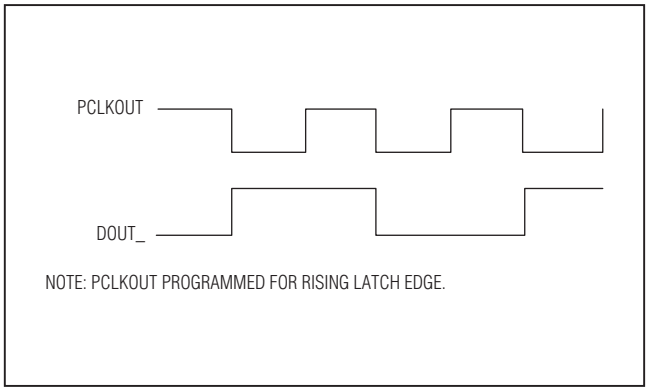


Figure 3. Worst-Case Pattern Output

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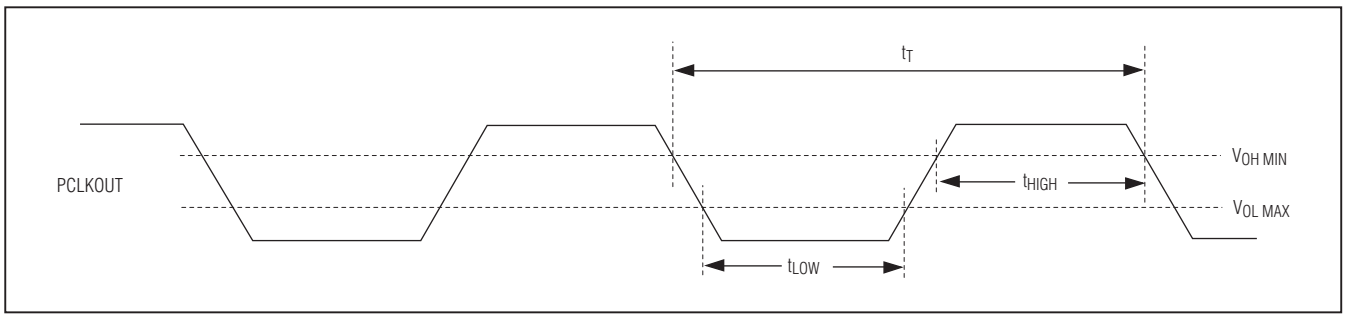

Figure 4. Clock Output High-and-Low Times

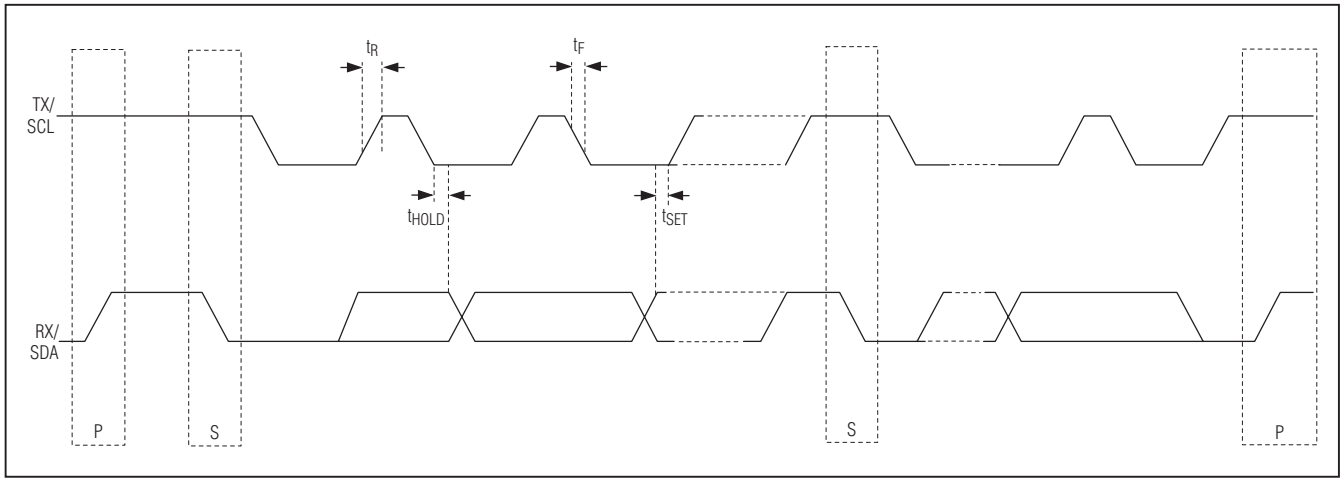

Figure 5. I²C Timing Parameters

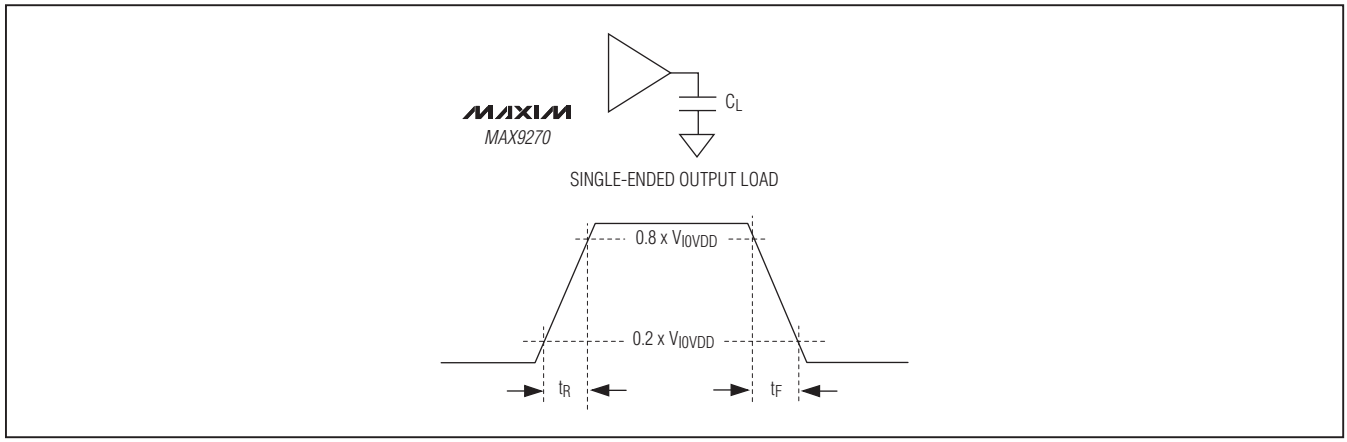

Figure 6. Output Rise-and-Fall Times

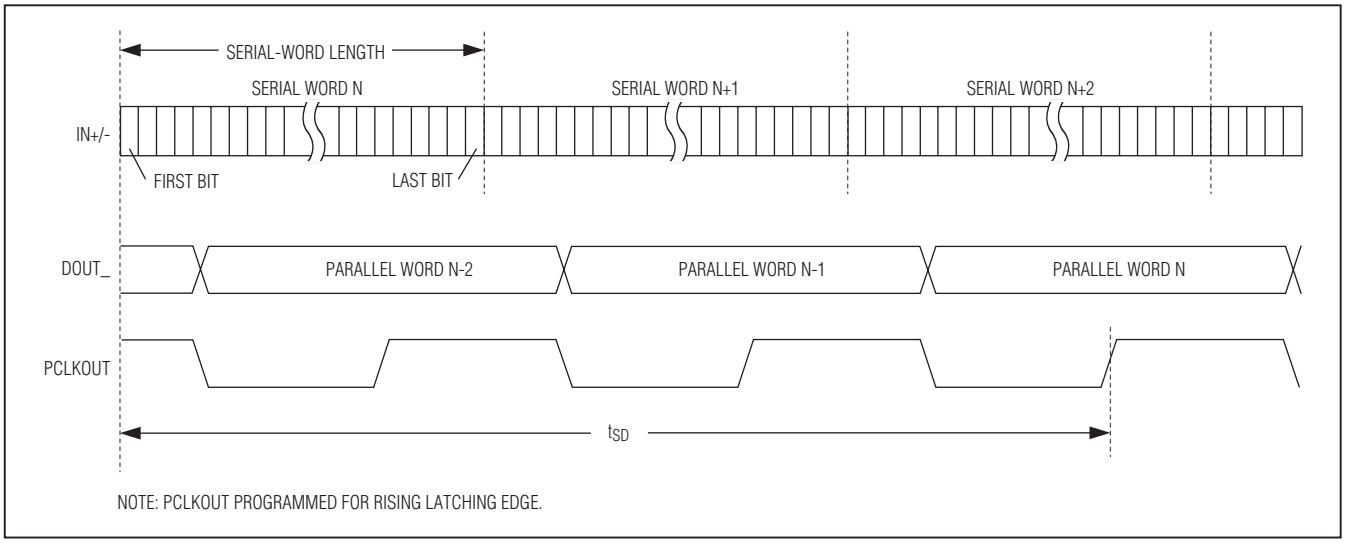

Figure 7. Deserializer Delay

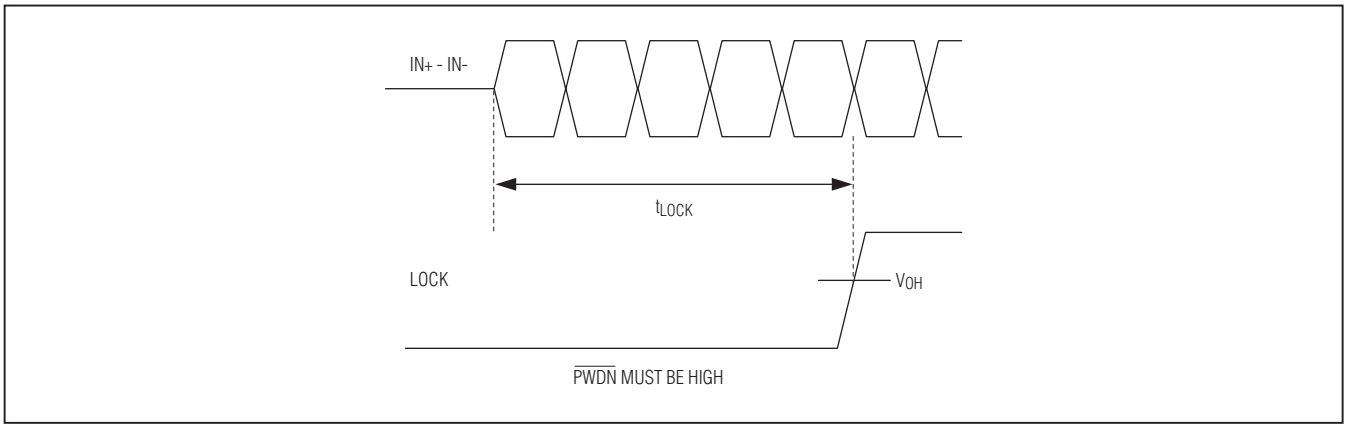

Figure 8. Lock Time

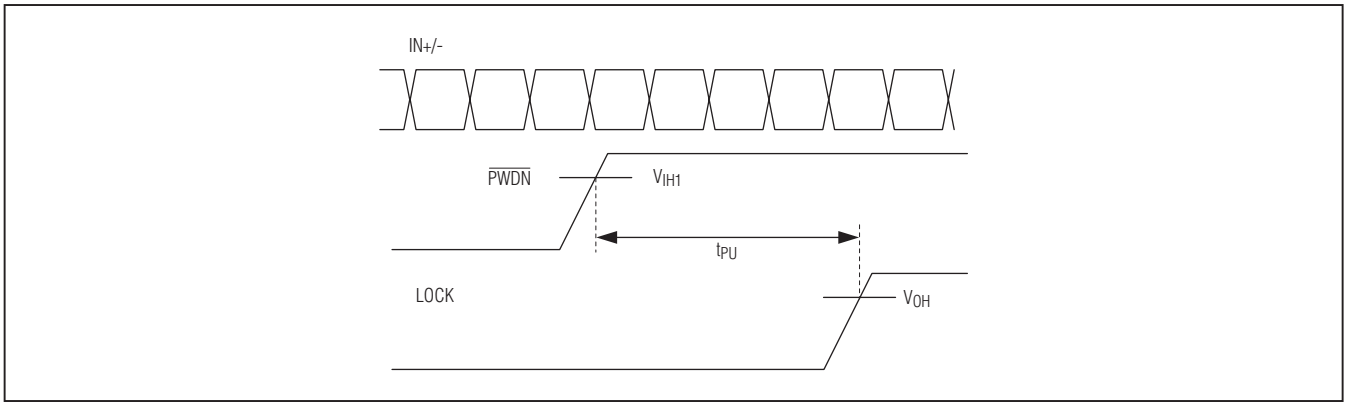

Figure 9. Power-Up Delay

Gigabit Multimedia Deserializer with Spread Spectrum and Full-Duplex Control Channel

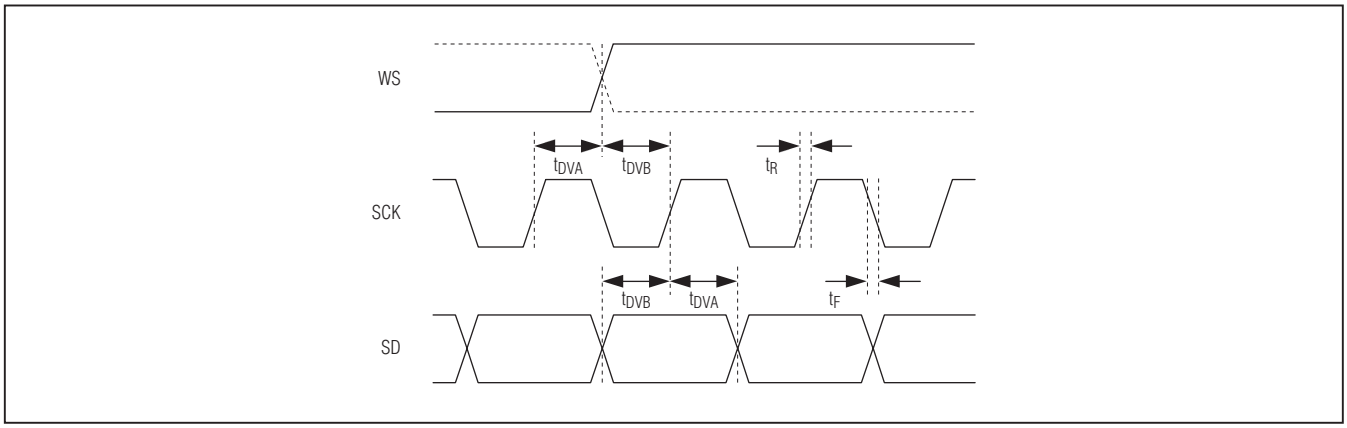

Figure 10. Output I²S Timing Parameters

Detailed Description

The MAX9270 deserializer utilizes Maxim's GMSL technology. This device pairs with any GMSL serializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data for video-display or image-sensing applications. The MAX9270 functions the same as the MAX9260 without an output enable pin ($\overline{ENABLE}$). Outputs are enabled by default and programmable by a register bit. The serial-payload data rate can reach up to 2.5Gbps for a 15m STP cable. The parallel interface is programmable for 24-bit or 32-bit width modes at the maximum bus clock of 104MHz or 78MHz, respectively. The minimum bus clock is 6.25MHz for the 32-bit mode and 8.33MHz for the 24-bit mode. With such a flexible data configuration, the GMSL is able to support XGA (1280 x 768) or dual-view WVGA (2 x 854 x 480) display panels. For image sensing, it supports three 10-bit camera links simultaneously with a pixel clock up to 78MHz. The 24-bit mode handles 21-bit data and control signals plus an I²S audio signal. The 32-bit mode handles 29-bit data and control signals plus an I²S audio signal. Any combination and sequence of color video data, video sync, and control signals make up the 21-bit or 29-bit parallel data on DOUT_. The I²S port supports the sampled audio data at a rate from 8kHz to 192kHz and the audio word length of anywhere between 4 to 32 bits. The embedded control channel forms a UART link between the serializer and deserializer. The UART link can be set to half-duplex mode or full-duplex mode depending on the application. The GMSL supports UART rates from 100kbps to 1Mbps. Using this control link, a host ECU or µC communicates with the serializer and deserializer, as well as the peripherals in the remote side, such as backlight control, grayscale gamma correction, camera module, and touch screen. All serial communication (forward and reverse) uses differential signaling. The peripheral programming uses I²C format or the default GMSL UART format. A separate bypass mode enables communication using a full-duplex, user-defined UART format. The control link between the serializer/deserializer allows µC connectivity to either device or peripherals to support video-display or image-sensing applications.

The AC-coupled serial link uses 8b/10b coding. The deserializer features a programmable channel equalizer to extend the link length and enhance the link reliability. A programmable spread-spectrum feature reduces EMI on the parallel data outputs. The differential serial link input pins comply with the ISO 10605 and IEC 61000-4-2 ESD-protection standards. This device uses a 3.3V core supply and a 1.8V to 3.3V I/O supply.

Register Mapping

The µC configures various operating conditions of the GMSL through registers in the serializer/deserializer. The default device addresses stored in the R0 and R1 registers of the serializer/deserializer are 0x80. Write to the R0/R1 registers to change the device address of the serializer or deserializer.

Table 1. Power-Up Default Register Map (see Table 12)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID =1000000, serializer device identifier is 1000 000 RESERVED = 0
0x01	0x90	DESID =1001000, deserializer device identifier is 1001 000 RESERVED = 0
0x02	0x1F or 0x5F	SS = 00 (SSEN = low), SS = 01 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up RESERVED = 0 AUDIOEN = 1, I^2S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking RESERVED = 0 SDIV = 00000, autocalibrate sawtooth divider
0x04	0x03 or 0x83	LOCKED = 0, LOCK output = low (read only) OUTENB = 0, outputs enabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, SLEEP setting default depends on CDS and MS pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I^2C REVCCEN = 1, reverse control channel active (sending) FWDCCEN = 1, forward control channel active (receiving)
0x05	0x28 or 0x29	RESERVED = 0 HPFTUNE = 01, 3.75MHz equalizer highpass cutoff frequency PDHF = 0, high-frequency boosting disabled EQTUNE = 1000 (EQS = high, 10.7dB), EQTUNE = 1001 (EQS = low, 5.2dB), EQTUNE default setting depends on EQS pin state at power-up
0x06	0x0F	DISSTAG = 0, staggered outputs enabled AUTORST = 0, error registers/output auto reset disabled DISINT = 0, INT transmission enabled INT = 0, INT output = low (read only) GPIO1OUT = 1, GPIO1 output set to high GPIO1 = 1, GPIO1 input = high (read only) GPIO0OUT = 1, GPIO0 output set to high GPIO0 = 1, GPIO0 input = high (read only)
0x07	0x54	RESERVED = 01010100
0x08	0x30	RESERVED = 00110000
0x09	0xC8	RESERVED = 11001000
0x0A	0x12	RESERVED = 00010010
0x0B	0x20	RESERVED = 00100000

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Table 1. Power-Up Default Register Map (see Table 12) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x0C	0x00	ERRTHR = 00000000, error threshold set to zero for decoding errors
0x0D	0x00 (read only)	DECERR = 00000000, zero decoding errors detected
0x0E	0x00 (read only)	PRBSERR = 00000000, zero PRBS errors detected
0x12	0x00	MCLKSRC = 0, MCLK is derived from PCLKOUT (see Table 4) MCLKDIV = 0000000, MCLK output is disabled
0x1E	0x02 (read only)	ID = 00000010, device ID is 0x02
0x1F	0x0X (read only)	RESERVED = 0000 REVISION = XXXX

Table 2. Bus-Width Selection Using BWS

BWS INPUT STATE	BUS WIDTH	PARALLEL BUS SIGNALS USED
Low	24	DOUT[0:20], WS, SCK, SD
High	32	DOUT[0:28], WS, SCK, SD

Parallel Outputs

The parallel bus uses two selectable bus widths, 24 bits and 32 bits. BWS selects the bus width according to Table 2. In 24-bit mode, DIN21–DIN28 are not used and are internally pulled down. For both modes, SD, SCK, and WS pins are dedicated for I²S audio data. The assignments of the first 21 or 29 signals are interchangeable and appear in the same order at both sides of the serial link. In image-sensing applications, disabling the I²S audio channel (through the internal registers) allows the serialization of three 10-bit camera data streams through DIN[0:28] plus SD inputs. The parallel bus accepts data clock rates from 8.33MHz to 104MHz for the 24-bit mode and 6.25MHz to 78MHz for the 32-bit mode.

Serial Link Signaling and Data Format

The serializer's high-speed data serial output uses CML signaling with programmable preemphasis and AC-coupling. The deserializer's high-speed receiver uses AC-coupling and programmable channel equalization. Together, the GMSL operates at up to 3.125Gbps over STP cable lengths up to 15m.

The serializer scrambles and encodes the parallel input bits, and sends the 8b/10b coded signal through the serial link. The deserializer recovers the embedded serial clock and then samples, decodes, and descrambles the data onto the parallel output bus. Figures 11 and 12 show the serial-data packet format prior to scrambling and 8b/10b coding. For the 24-bit or 32-bit mode, the first 21 or 29 serial bits map to DOUT[20:0] or DOUT[28:0], respectively. The audio channel bit (ACB) contains an encoded audio signal derived from the three I²S inputs (SD, SCK, and WS). The forward control channel (FCC) bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

Reverse Control Channel

The GMSL uses the reverse control channel to send I²C/UART in the opposite direction of the video stream from the deserializer to the serializer. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Parallel Data-Rate Selection

The deserializer uses the DRS input to set the parallel data rate. Set DRS high to use a low-speed parallel data rate in the range of 6.25MHz to 12.5MHz (32-bit mode) or 8.33MHz to 16.66MHz (24-bit mode). Set DRS low

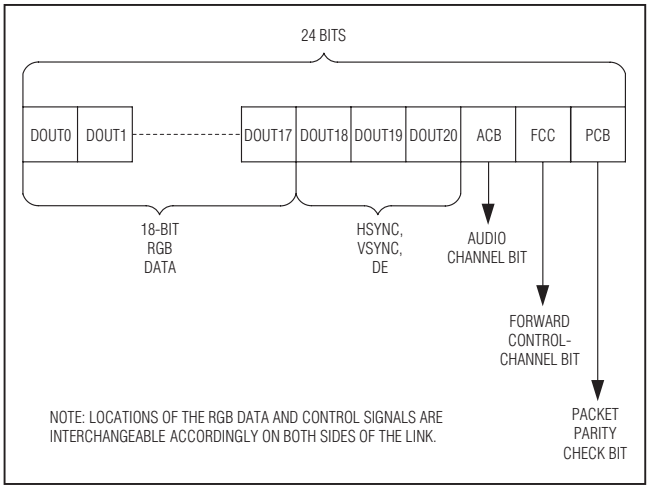

Figure 11. 24-Bit Mode Serial Link Data Format

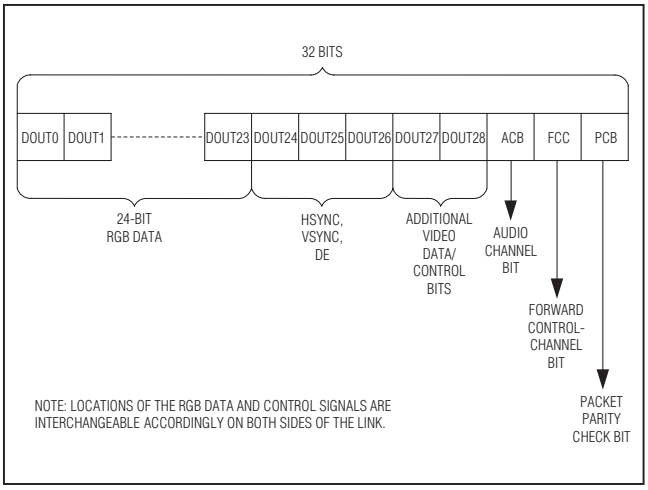

Figure 12. 32-Bit Mode Serial Link Data Format

Table 3. Maximum Audio Sampling Rates for Various PCLK_ Frequencies

WORD LENGTH (Bits)	PCLK_ FREQUENCY (DRS = LOW) (MHz)				PCLK_ FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

for normal operation with parallel data rates higher than 12.5MHz (32-bit mode) or 16.66MHz (24-bit mode).

Audio Channel

The I²S audio channel supports audio sampling rates from 8kHz to 192kHz and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not need to be synchronized with PCLKIN. The serializer automatically encodes audio data into a single bit stream synchronous with PCLKIN. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, the SD pins on both sides are treated as a regular parallel data pin.

PCLK_ frequencies can limit the maximum supported audio sampling rate. Table 3 lists the maximum audio sampling rate for various PCLK_ frequencies. Spread-spectrum settings do not affect the I²S data rate or WS clock frequency.

Additional MCLK Output for Audio Applications

Some audio DACs such as the MAX9850 do not require a synchronous main clock (MCLK), while other DACs require MCLK to be a specific multiple of WS. If an audio DAC chip needs the MCLK to be a multiple of WS, synchronize the I²S audio data with PCLK_ of the GMSL, which is typical for most applications. Select the PCLK_ to be the multiple of WS, or use a clock synthesis chip, such as the MAX9491, to regenerate the required MCLK from PCLK_ or SCK.

For audio applications that cannot directly use the PCLKOUT output, the deserializer provides a divided MCLK output on DOUT28 at the expense of one less parallel line in 32-bit mode (24-bit mode is not affected). By default, DOUT28 operates as a parallel data output and

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Table 4. f_{SRC} Settings

MCLKSRC SETTING (REGISTER 0x12, D7)	DATA-RATE SETTING	BIT-WIDTH SETTING	MCLK SOURCE FREQUENCY (f_{SRC})
0	High speed	24-bit mode	3 x $f_{PCLKOUT}$
		32-bit mode	4 x $f_{PCLKOUT}$
	Low speed	24-bit mode	6 x $f_{PCLKOUT}$
		32-bit mode	8 x $f_{PCLKOUT}$
1	—	—	Internal oscillator (120MHz typ)

MCLK is turned off. Set MCLKDIV (deserializer register 0x12, D[6:0]) to a non-zero value to enable the MCLK output. Set MCLKDIV to 0x00 to disable MCLK and set DOUT28 as a parallel data output.

The output MCLK frequency is:

$$f_{MCLK} = \frac{f_{SRC}}{MCLKDIV}$$

where f_{SRC} is the MCLK source frequency (Table 4) and MCLKDIV is the divider ratio from 1 to 127.

Choose MCLKDIV values so that f_{MCLK} is not greater than 60MHz. MCLK frequencies derived from PCLK_ (MCLKSRC = 0) are not affected by spread-spectrum settings in the deserializer. Enabling spread spectrum in the serializer, however, introduces spread spectrum into MCLK. Spread-spectrum settings of either device do not affect MCLK frequencies derived from the internal oscillator. The internal oscillator frequency ranges from 100MHz to 150MHz over all process corners and operating conditions.

Control-Channel and Register Programming

The µC uses the control link to send and receive control data over the STP link simultaneously with the high-speed data. Configuring the CDS pin allows the µC to control the link from either the serializer or the deserializer side to support video-display or image-sensing applications.

The control link between the µC and the serializer/deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control link and the bypass mode is a full-duplex control link. In base mode, the µC is the host and accesses the registers of both the serializer/deserializer by using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets converted to I^2C by the device on the remote side of the link (deserializer for LCD or serializer for image-sensing applications). The µC communicates with a UART peripheral in base mode (through INTTYPE register settings) using the half-duplex default GMSL UART protocol. The device addresses of the serializer and deserializer in the base mode are programmable. The default values are 0x80 and 0x90, respectively.

In base mode, when the peripheral interface uses I^2C (default), the serializer/deserializer only convert packets that have device addresses different from themselves to I^2C. The converted I^2C bit rate is the same as the original UART bit rate.

In bypass mode, the µC bypasses the GMSL and communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the GMSL registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLK_ period of jitter due to the asynchronous sampling of the UART signal by PCLK_.

The serializer embeds control signals going to the deserializer in the high-speed forward link. Do not send a low value longer than 100µs in either base or bypass mode. The deserializer uses a proprietary differential line coding to send signals back towards the serializer. The speed of the control link ranges from 100kbps to 1Mbps in both directions. The serializer/deserializer automatically detects the control-channel bit rate in base mode. Packet bit rates can vary up to 3.5x from the previous bit rate (see the *Changing the Data Frequency* section). Figure 13 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 14 shows the UART data format. Even parity is used. Figures 15 and 16 detail the formats of the SYNC byte (0x79) and ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK

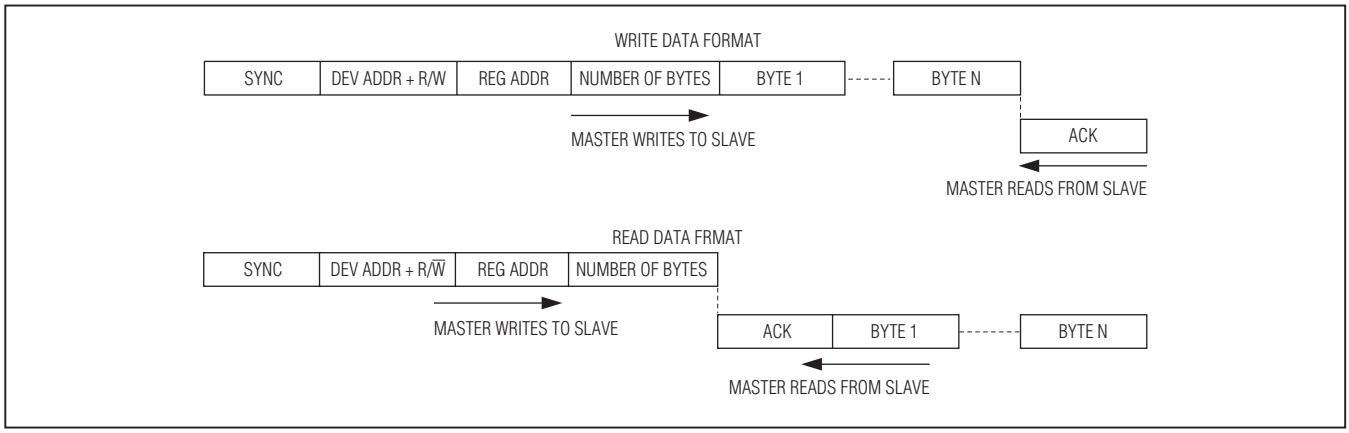

Figure 13. UART Protocol for Base Mode

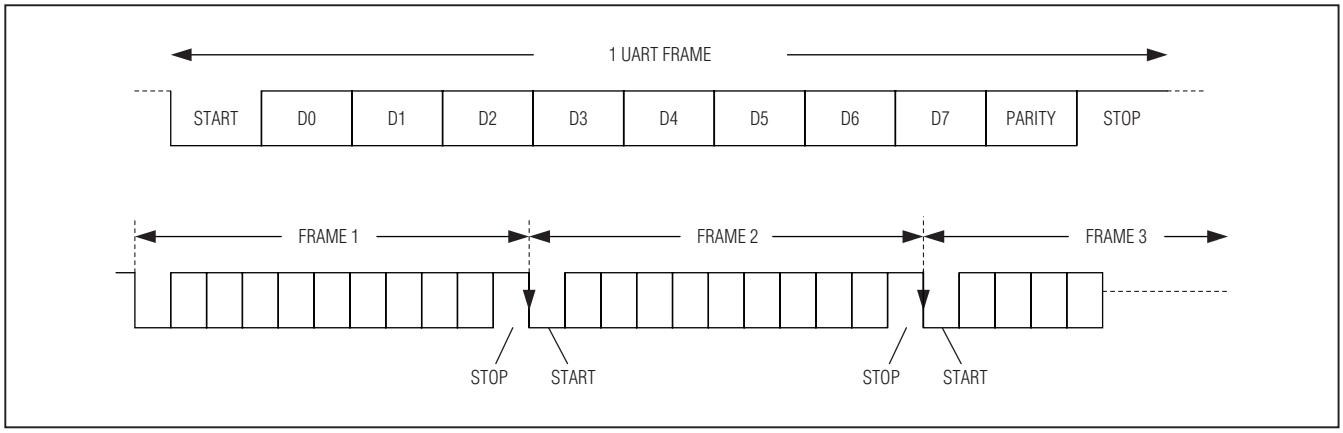

Figure 14. UART Data Format for Base Mode

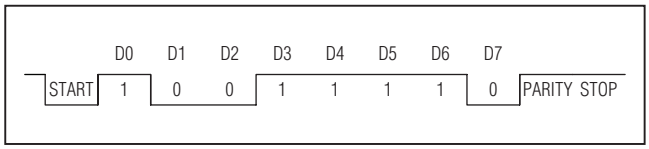

Figure 15. SYNC Byte (0x79)

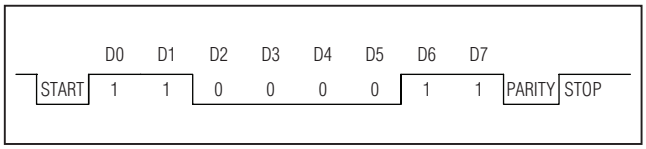

Figure 16. ACK Byte (0xC3)

byte, respectively. Certain events such as device wake-up and interrupt generate signals on the control path and should be ignored by the µC. All data written to the internal registers do not take affect until after the acknowledge byte is sent. This allows the µC to verify that write commands are processed without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART data rate automatically. If the INT or MS inputs of the device toggle while there is control-channel communication, the control-channel communication can be corrupted. In the event of a missed acknowledge, the µC should assume there was an error in the packet when the slave device receives it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit times before starting to send a new packet.

As shown in Figure 17, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C's data rate is the same as the UART data rate.

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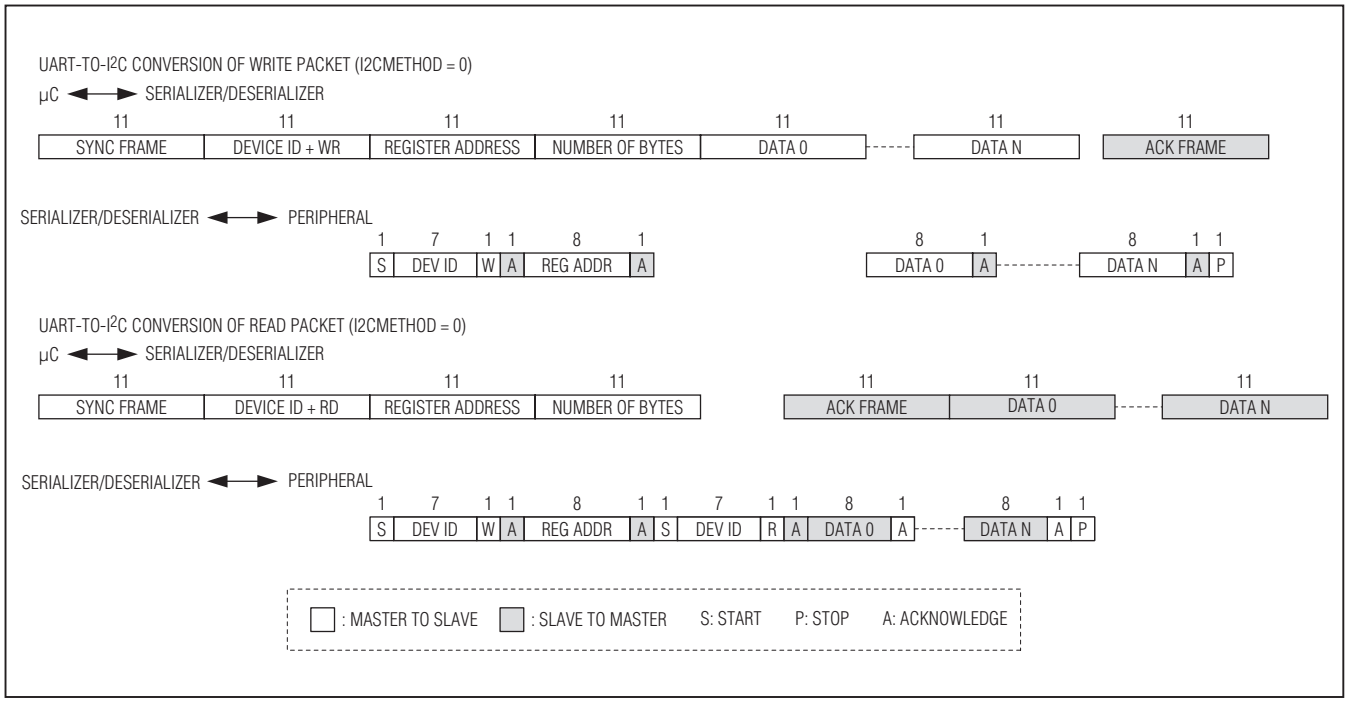

Figure 17. Format Conversion between UART and I²C with Register Address (I2CMETHOD = 0)

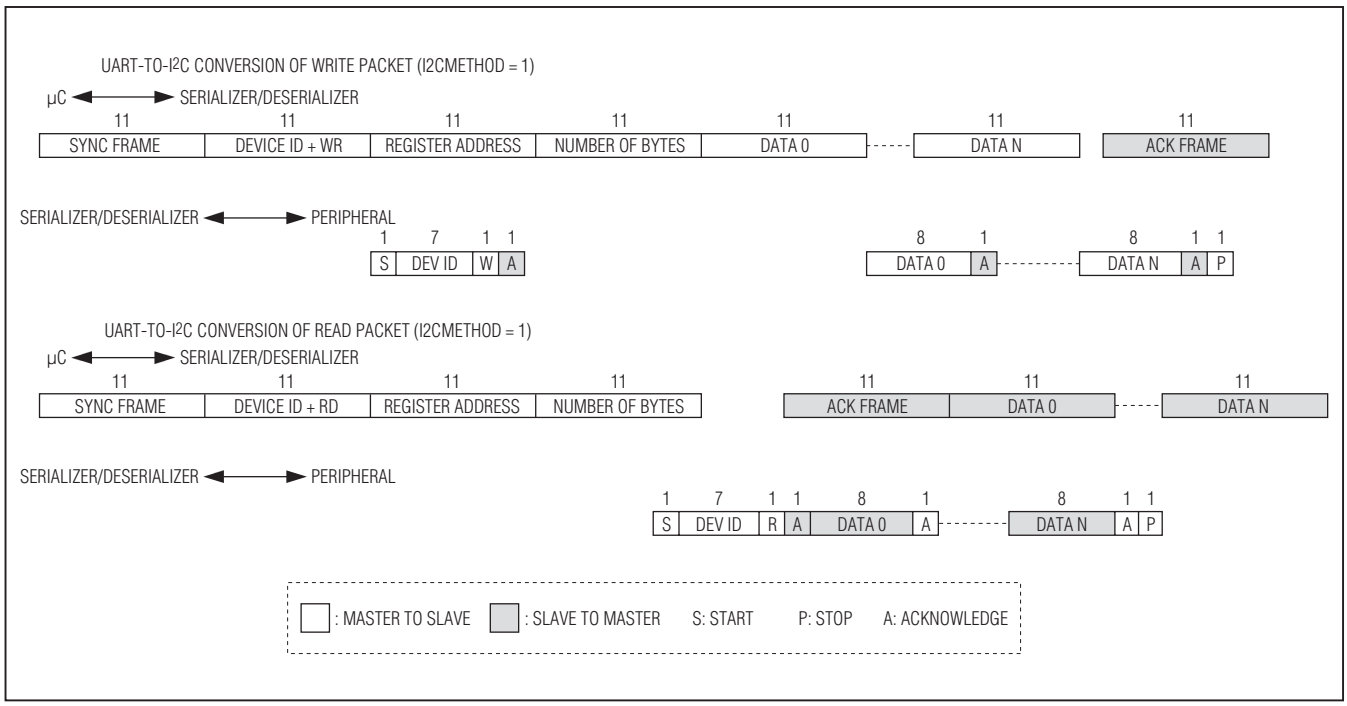

Figure 18. Format Conversion between UART and I²C in Command-Byte-Only Mode (I2CMETHOD = 1)

Interfacing Command-Byte-Only I²C Devices

The GMSL UART-to-I²C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 18).

Interrupt Control

The INT of the serializer is the interrupt output and the INT of the deserializer is the interrupt input. The interrupt output on the serializer follows the transitions at the interrupt input of the deserializer. This interrupt function supports remote-side functions such as touch-screen peripherals, remote power-up, or remote monitoring. Interrupts that occur during periods where the reverse control channel is disabled, such as link startup/shutdown, are automatically resent once the reverse control channel becomes available again. Bit D4 of register 0x06 in the deserializer also stores the interrupt input state. Writing to the SETINT register bit also sets the INT output of the serializer. In addition, the µC sets the INT output of the serializer by writing to the SETINT register bit. In normal operation, the state of the interrupt output changes when the interrupt input on the deserializer toggles.

Line Equalizer

The deserializer includes an adjustable line equalizer to further compensate cable attenuation at high frequencies. The cable equalizer has 11 selectable levels of compensation from 2.1dB to 13dB (Table 5). The EQS input selects the default equalization level at power-up. The state of EQS is latched upon power-up or when resuming from power-down mode. To select other equalization levels, set the corresponding register bits in the deserializer (0x05 D[3:0]). Use equalization in the deserializer, together with preemphasis in the serializer to create the most reliable link for a given cable.

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link and parallel outputs, the deserializer supports spread spectrum. Turning on spread spectrum on the deserializer spreads the parallel video outputs. Do not enable spread spectrum for both the serializer and deserializer. The two selectable spread-spectrum rates at the parallel outputs are ±2% and ±4% (Table 6).

Set the SSEN input high to select 2% spread at power-up and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode.

Turning on spread spectrum does not affect the audio data stream. Changes in the serializer spread settings only affect MCLK output if it is derived from PCLK_ (MCLKSRC = 0).

Table 5. Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2 **Power-up default (EQS = high)**
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	10.7 **Power-up default (EQS = low)**
1010	11.7
1011	13

Table 6. Parallel Output Spread

SS	SPREAD (%)
00	No spread spectrum. **Power-up default when SSEN = low.**
01	±2% spread spectrum. **Power-up default when SSEN = high.**
10	No spread spectrum.
11	±4% spread spectrum.

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The device includes a sawtooth divider to control the spread-modulation rate. Autodetection or manual programming of the PCLK_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV, 0x03 D[5:0]) allows the user to set a specific modulation frequency for a specific PCLK_ rate. Always keep the modulation frequency between 20kHz to 40kHz to ensure proper operation.

Manual Programming of the Spread-Spectrum Divider

The modulation rate relates to the PCLK_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{PCLK\_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency.

DRS = DRS pin input value (0 or 1).

$f_{PCLK\_}$ = Parallel clock frequency (12.5MHz to 104MHz).

MOD = Modulation coefficient given in Table 7.

SDIV = 5-bit SDIV setting, manually programmed by the µC.

To program the SDIV setting, first look up the modulation coefficient according to the part number and desired bit-width and spread-spectrum settings. Solve the above equation for SDIV using the desired parallel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 7, set SDIV to the maximum value.

Sleep Mode

The deserializer includes a low-power sleep mode to reduce power consumption when it is not attached to the µC LCD applications. Set the SLEEP bit to 1 to initiate sleep mode. The deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC side device cannot enter into sleep mode, and its SLEEP bit remains at 0. Use the $\overline{PWDN}$ input pin to bring the µC side device into a low-power state.

Configuration Link Mode

The GMSL includes a low-speed configuration link to allow control-data connection between the two devices in the absence of a valid parallel clock input. In either display or camera applications, the configuration link can be used to program equalizer/preemphasis or other registers before establishing the video link. An internal oscillator provides PCLK_ for establishing the serial configuration link between the serializer and deserializer. The parallel output clock and data lines are disabled in the deserializer. The LOCK output remains low even after a successful configuration link lock. Set CLINKEN = 1 on the serializer to turn on the configuration link. The configuration link remains active as long as the video link has not been enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 8 lists four startup cases for video-display applications. Table 9 lists two startup cases for image-sensing applications. In either display or image-sensing applications, the control link is always available after the high-speed data link or the configuration link is established and the GMSL registers or the peripherals are ready for programming.

Video-Display Applications

For the video-display application, with a remote display unit, connect the µC to the serializer and set CDS = low for both the serializer and deserializer. Table 8 summarizes the four startup cases based on the settings of $\overline{AUTOS}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the serializer and deserializer, the serial link establishes if a stable PCLK_ is present. The serializer locks to PCLK_ and sends the serial data to the deserializer. The deserializer then detects activity on the serial link and locks to the input serial data.

Table 7. Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (decimal)	SDIV UPPER LIMIT (decimal)
4	208	15
2	208	30

Table 8. Startup Selection for Video-Display Applications (CDS = Low)

CASE	$\overline{\text{AUTOS}}$ (SERIALIZER)	SERIALIZER POWER-UP STATE	MS (DESERIALIZER)	DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with the serial link active (autostart).
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	Serial link is disabled and the deserializer powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the serializer to start the serial link and wake up the deserializer.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link disabled. Set SEREN = 1 or CLINKEN = 1 in the serializer to start the serial link.
4	Low	Serialization enabled	High	Sleep mode (SLEEP = 1)	The deserializer starts in sleep mode. Link autostarts upon the serializer power-up. Use this case when the deserializer powers up before the serializer.

Case 2: Standby Start Mode

After power-up, or when $\overline{\text{PWDN}}$ transitions from low to high for both the serializer and deserializer, the deserializer starts up in sleep mode, and the serializer stays in standby mode (does not send serial data). Use the µC and program the serializer to set SEREN = 1 to establish a video link or CLINKEN = 1 to establish the configuration link. After locking to a stable PCLK_ (for SEREN = 1) or the internal oscillator (for CLINKEN = 1), the serializer sends a wake-up signal to the deserializer. The deserializer exits sleep mode after locking to the serial data and sets SLEEP = 0. If after 8ms the deserializer does not lock to the input serial data, the deserializer goes back to sleep, and the internal sleep bit remains uncleared (SLEEP = 1).

Case 3: Remote Side Autostart Mode

After power-up, or when $\overline{\text{PWDN}}$ transitions from low to high, the remote device (deserializer) starts up and tries to lock to an incoming serial signal with sufficient power. The host side (serializer) is in standby mode and does not try to establish a link. Use the µC and program the serializer to set SEREN = 1 (and apply a stable PCLK_) to establish a video link, or CLINKEN = 1 to establish the configuration link. In this case, the deserializer ignores the short wake-up signal sent from the serializer.

Case 4: Remote Side in Sleep Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high, the remote device (deserializer) starts up in sleep mode. The high-speed link establishes automatically after the serializer powers up with a stable PCLK_ and sends a wake-up signal to the deserializer. Use this mode in applications where the deserializer powers up before the serializer.

Image-Sensing Applications

For image-sensing applications, with remote camera unit(s), connect the µC to the deserializer and set CDS = high for both the serializer and deserializer. The deserializer powers up normally (SLEEP = 0) and continuously tries to lock to a valid serial input. Table 9 summarizes the two startup cases, based on the state of the serializer $\overline{\text{AUTOS}}$ pin.

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Table 9. Startup Selection for Image-Sensing Applications (CDS = High)

CASE	$\overline{\text{AUTOS}}$ (SERIALIZER)	SERIALIZER POWER-UP STATE	DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Normal (SLEEP = 0)	Autostart.
2	High	Sleep mode (SLEEP = 1)	Normal (SLEEP = 0)	Serializer is in sleep mode. Wake up the serializer through the control channel (µC attached to the deserializer).

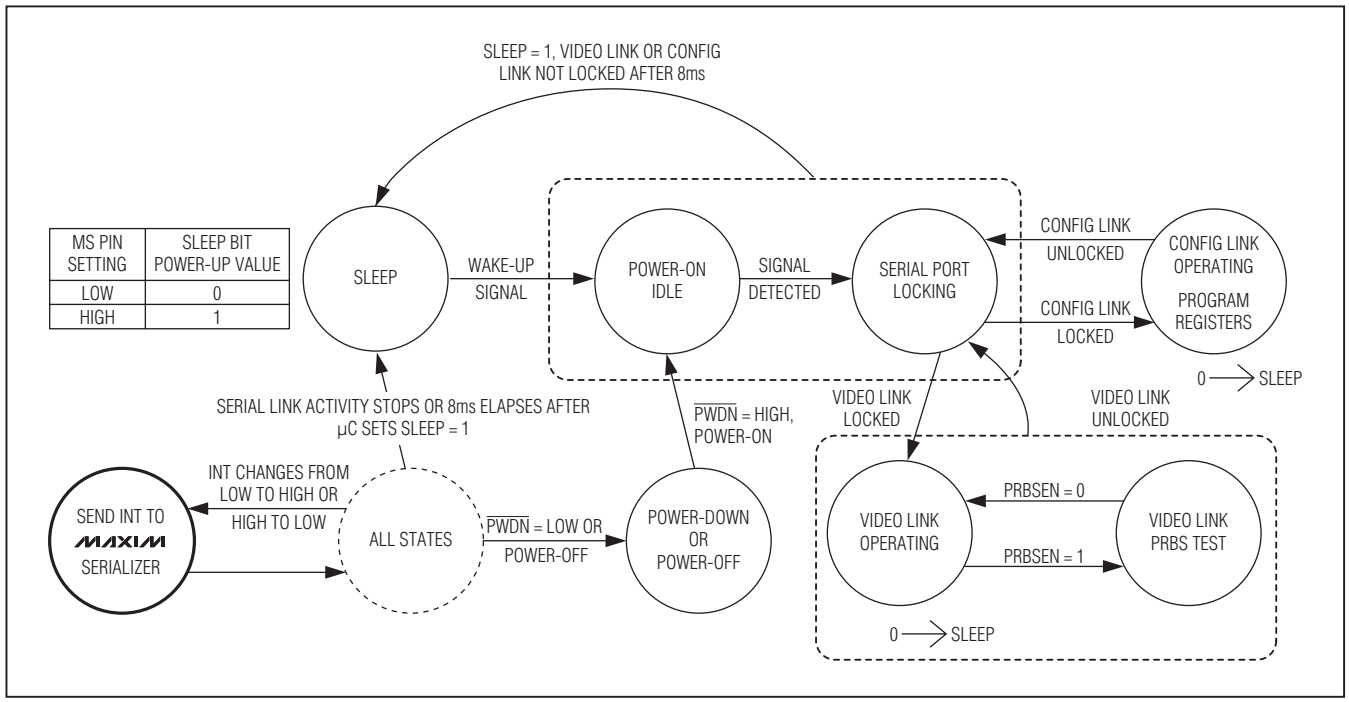

Figure 19. State Diagram, CDS = Low (LCD Application)

Case 1: Autostart Mode

After power-up, or when $\overline{\text{PWDN}}$ transitions from low to high, the serializer locks to a stable PCLKIN and sends the high-speed data to the deserializer. The deserializer locks to the serial data and outputs the parallel video data and PCLKOUT.

Case 2: Sleep Mode

After power-up, or when $\overline{\text{PWDN}}$ transitions from low to high, the serializer starts up in sleep mode. To wake up the serializer, use the µC to send a regular UART frame containing at least three rising edges (e.g., 0x66), at a bit rate no greater than 1Mbps. The low-power wake-up receiver of the serializer detects the wake-up frame over the reverse control channel and powers up. Reset the sleep bit (SLEEP = 0) of the serializer using a regular control-channel write packet to power up the device fully. Send the sleep bit write packet at least 500µs after the wake-up frame. The serializer goes back to sleep mode if its sleep bit is not cleared within 8ms (typ) after detecting a wake-up frame.

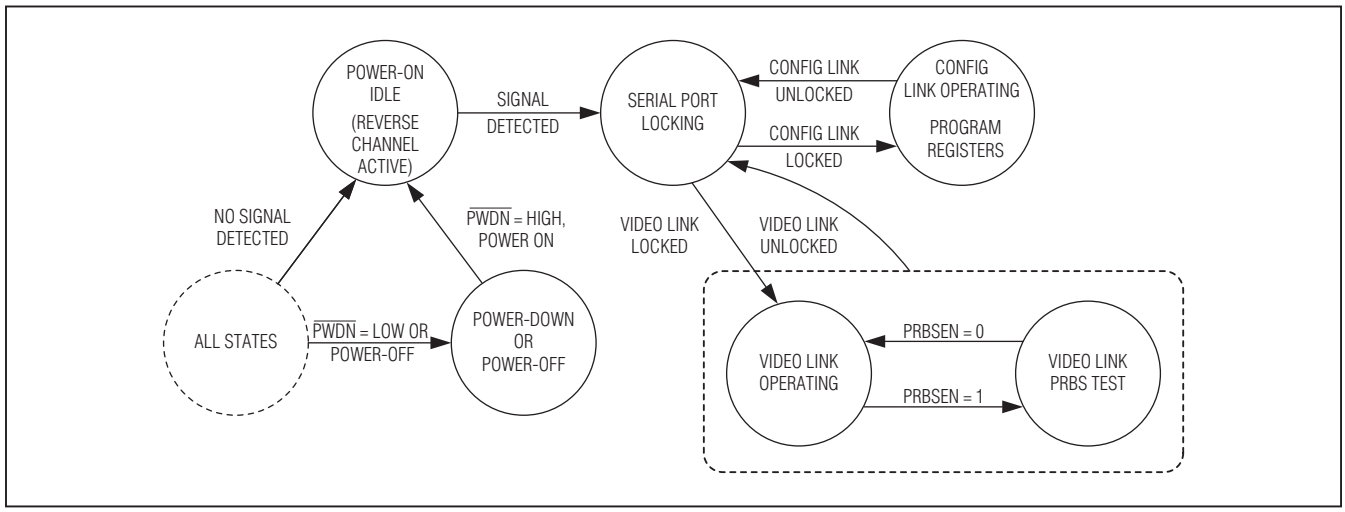

Figure 20. State Diagram, CDS = High (Camera Application)

Applications Information

Error Checking

The deserializer checks the serial link for errors and stores the number of detected decoding errors in the 8-bit register (DECERR, 0x0D). If a large number of decoding errors are detected within a short duration, the deserializer loses lock and stops the error counter. The deserializer then attempts to relock to the serial data. DECERR resets upon successful video link lock, successful readout of DECERR (through UART), or whenever auto-error reset is enabled. The deserializer does not check for decoding errors during the internal PRBS test and DECERR is reset to 0x00.

$\overline{ERR}$ Output

The deserializer has an open-drain $\overline{ERR}$ output. This output asserts low whenever the number of decoding errors exceed the error threshold (ERRTHR, 0x0C) during normal operation, or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ reasserts high whenever DECERR (0x0D) resets, due to DECERR readout, video link lock, or autoerror reset.

Autoerror Reset

The default method to reset errors is to read the respective error registers in the deserializer (0x0D, 0x0E). Autoerror reset clears the decoding-error counter (DECERR) and the $\overline{ERR}$ output ~1µs after $\overline{ERR}$ goes low. Autoerror reset is disabled on power-up. Enable autoerror reset through AUTORST (0x06 D6). Autoerror reset does not run when the device is in PRBS test mode.

Self PRBS Test

The GMSL link includes a PRBS pattern generator and bit-error verification function. Set PRBSEN = 1 (0x04 D5) first in the serializer and then the deserializer to start the PRBS test. Set PRBSEN = 0 (0x04 D5) first in the deserializer and then the serializer to exit the PRBS self test. The deserializer uses an 8-bit register (0x0E) to count the number of detected errors. The control link also controls the start and stop of the error counting. During PRBS mode, the device does not count decoding errors and the $\overline{ERR}$ output reflects PRBS errors only. Autoerror reset does not run when the device is in PRBS mode.

Microcontrollers on Both Sides of the GMSL Link (Dual µC Control)

Usually the µC is either on the serializer side for video-display applications, or on the deserializer side for image-sensing applications. For the former case, both the CDS pins are set to low, and for the latter case, the CDS pins are set to high. However, if the CDS pin of the serializer is low and the CDS pin of the deserializer is high, then the serializer/deserializer can both connect to µCs simultaneously. In such a case, the µCs on either side can communicate with the GMSL UART protocol.

Contentions of the control link may happen if the µCs on both sides are using the link at the same time. The GMSL does not provide the solution for contention avoidance. The serializer/deserealizer do not send an acknowledge frame when communication fails due to contention. Users can always implement a higher-layer protocol to

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avoid the contention. In addition, if UART communication across the serial link is not required, the µCs can disable the forward and reverse control channel through the FWDCCEN and REVCCEN bits (0x04 D[1:0]) in the devices. UART communication across the serial link is stopped and contention between µCs no longer occurs. During the dual µC operation, if one of the CDS pins on either side changes state, the link resumes the corresponding state described in the *Link Startup Procedure* section.

As an example of dual µC use in an image-sensing link, the serializer may be in sleep mode and waiting to be waked up by the deserializer. After wake-up, the serializer-side µC sets the serializer CDS pin low and assumes master control of the serializer registers.

Changing the Data Frequency

Both the video data rate ($f_{PCLK\_}$) and the control data rate (f_{UART}) can be changed on-the-fly to support applications with multiple clock speeds. Slow speed/performance modes allow significant power savings when a system's full capabilities are not required. Enable the GMSL link after PCLK_ stabilizes. Stop PCLKIN for 5µs and restart the serial link or toggle SEREN after each change in the parallel clock frequency to recalibrate any automatic settings if a clean frequency change cannot be guaranteed. The reverse control channel remains unavailable for 350µs after serial link start or stop. Limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps to have reduction ratios of 3 and 3.333, respectively.

LOCK Output Loopback

Connect the LOCK output to the INT input of the device to loopback LOCK to the serializer. The interrupt output on the serializer follows the transitions at the LOCK output of the deserializer. Reverse-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the video link. LOCK asserts for video link only and not for the configuration link.

GPIOs

The device has two open-drain GPIOs available. GPIO1OUT and GPIO0OUT (0x06 D3, D1) set the output state of the GPIOs. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x06 D2, D0). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Staggered Parallel Data Outputs

The device staggers the parallel data outputs to reduce EMI and noise. Staggering outputs also reduce the power-supply transient requirements. By default, the deserializer staggers outputs according to Table 10. Disable output staggering through the DISSTAG bit (0x06 D7)

Choosing I²C/UART Pullup Resistors

Both I²C/UART open-drain lines require pullup resistors to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. The waveforms are not recognized if the transition time becomes too slow. The device supports I²C/UART rates up to 1Mbps.

Table 10. Staggered Output Delay

OUTPUT	OUTPUT DELAY RELATIVE TO DOUT0 (ns)	
	DISSTAG = 0	DISSTAG = 1
DOUT0–DOUT5, DOUT21, DOUT22	0	0
DOUT6–DOUT10, DOUT23, DOUT24	0.5	0
DOUT11–DOUT15, DOUT25, DOUT26	1	0
DOUT16–DOUT20, DOUT27, DOUT28	1.5	0
PCLKOUT	0.75	0

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Four capacitors—two at the serializer output and two at the deserializer input—are needed for proper link operation and to provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML receiver termination resistor (R_{TR}), the CML driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. Use at least 0.2µF (100V) high-frequency surface-mount ceramic capacitors to pass the lower speed reverse-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The device uses an AVDD and DVDD of 3.0V to 3.6V. All single-ended inputs and outputs on the device derive power from an IOVDD of 1.7V to 3.6V. The input levels or output levels scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic-field canceling effects. Balanced cables pick up noise as common mode rejected by the CML receiver. Table 11 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate the parallel signals and CML high-speed serial signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML, and digital signals. Layout PCB traces close to each other and have a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer.

Route the PCB traces for a CML channel (there are two conductors per CML channel) in parallel to maintain the differential characteristic impedance. Avoid vias. If vias must be used, use only one pair per CML channel and place the via for each line at the same point along the length of the PCB traces. This way, any reflections occur at the same time. Do not make vias into test points for ATE. Keep PCB traces that make up a differential pair equal in length to avoid skew within the differential pair.

Table 11. Suggested Connectors and Cables for GMSL

SUPPLIER	CONNECTOR	CABLE
JAE Electronics, Inc.	MX38-FF	A-BW-Lxxxxx
Nissei Electric Co., Ltd.	GT11L-2S	F-2WME AWG28
Rosenberger Hochfrequenztechnik GmbH	D4S10A-40ML5-Z	Dacar 538

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ESD Protection

The ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. Serial inputs meet ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All other pins meet the Human Body Model ESD tolerances. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 21). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 22). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 23).

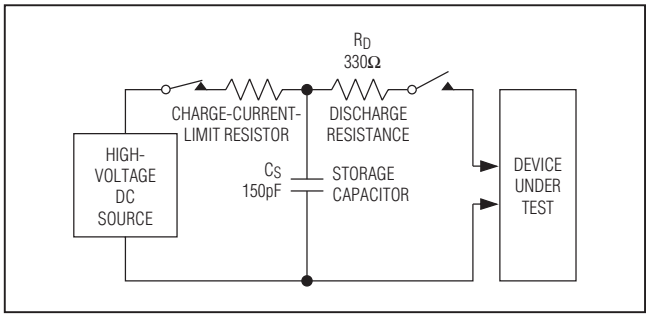

Figure 22. IEC 61000-4-2 Contact Discharge ESD Test Circuit

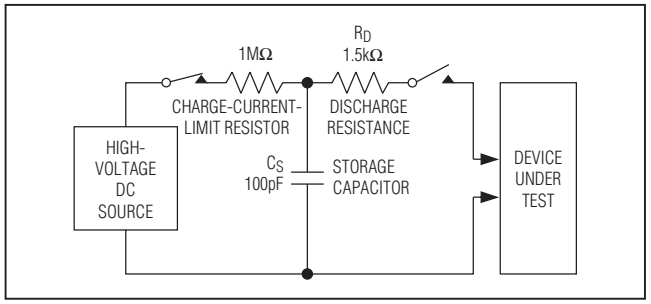

Figure 21. Human Body Model ESD Test Circuit

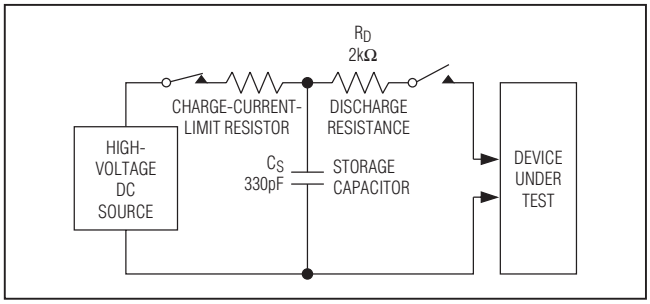

Figure 23. ISO 10605 Contact Discharge ESD Test Circuit

Table 12. Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address.	1000000
	D0	—	0	Reserved.	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address.	1001000
	D0	—	0	Reserved.	0
0x02	D[7:6]	SS	**00**	No spread spectrum. **Power-up default when SSEN = low**.	00, 01
			01	±2% spread spectrum. **Power-up default when SSEN = high**.	
			10	No spread spectrum.	
			11	±4% spread spectrum.	
	D5	—	0	Reserved.	0
	D4	AUDIOEN	0	Disable I²S channel.	1
			1	Enable I²S channel.	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock.	11
			01	25MHz to 50MHz pixel clock.	
			10	50MHz to 104MHz pixel clock.	
			11	Automatically detect the pixel clock range.	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial-data rate.	11
			01	1 to 2Gbps serial-data rate.	
			10	2 to 3.125Gbps serial-data rate.	
			11	Automatically detect serial-data rate.	

Table 12. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking.	00
			01	Calibrate spread-modulation rate every 2ms after locking.	
			10	Calibrate spread-modulation rate every 16ms after locking.	
			11	Calibrate spread-modulation rate every 256ms after locking.	
	D5	—	0	Reserved.	0
	D[4:0]	SDIV	00000	Autocalibrate sawtooth divider.	00000
			XXXXX	Manual SDIV setting (see the *Manual Programming of the Spread-Spectrum Divider* section).	
0x04	D7	LOCKED	0	LOCK output is low.	0 (read only)
			1	LOCK output is high.	
	D6	OUTENB	0	Enable outputs.	0
			1	Disable outputs.	
	D5	PRBSEN	0	Disable PRBS test.	0
			1	Enable PRBS test.	
	D4	SLEEP	0	Normal mode default value depends on CDS and MS pin values at power-up).	0, 1
			1	Activate sleep mode default value depends on CDS and MS pin values at power-up).	
	D[3:2]	INTTYPE	00	Base mode uses I^2C peripheral interface.	00
			01	Base mode uses UART peripheral interface.	
			10, 11	Base mode peripheral interface disabled.	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending).	1
			1	Enable reverse control channel to serializer (sending).	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving).	1
			1	Enable forward control channel from serializer (receiving).	

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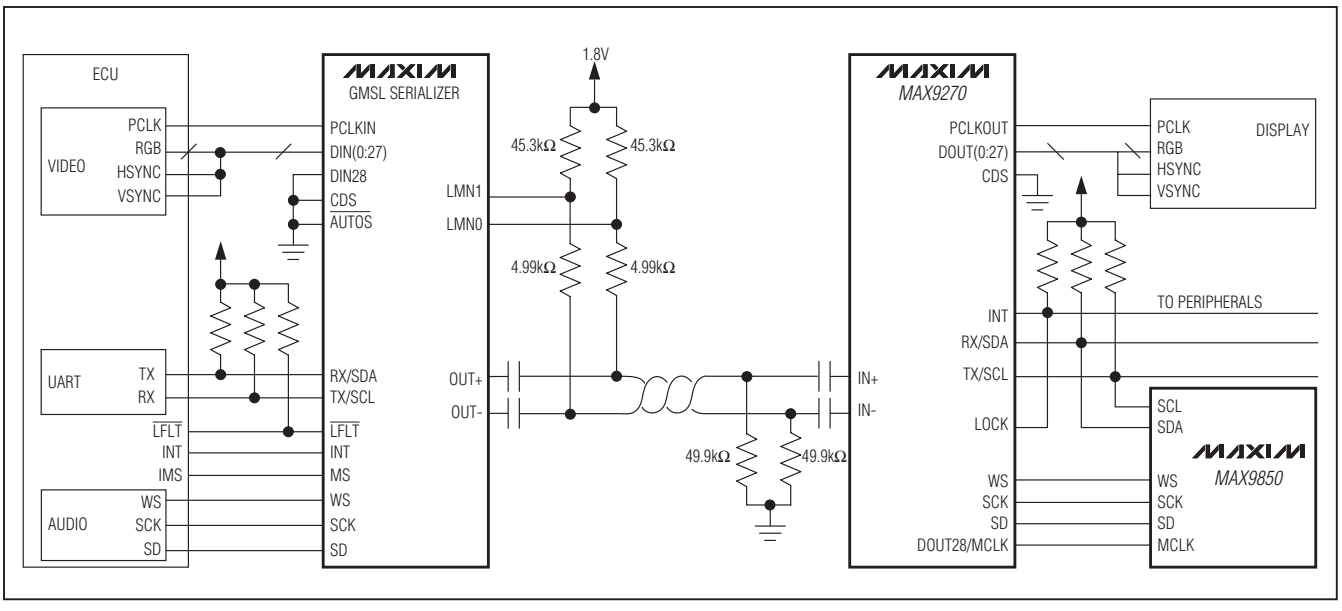
Table 12. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address.	0
			1	Disable sending of I²C register address (command-byte-only mode).	
	D[6:5]	HPFTUNE	00	7.5MHz Equalizer highpass cutoff frequency.	01
			01	3.75MHz cutoff frequency.	
			10	2.5MHz cutoff frequency.	
			11	1.87MHz cutoff frequency.	
	D4	PDHF	0	High-frequency boosting enabled.	0
			1	High-frequency boosting disabled.	
	D[3:0]	EQTUNE	0000	2.1dB equalizer boost gain.	0100, 1001
			0001	2.8dB equalizer boost gain.	
			0010	3.4dB equalizer boost gain.	
			0011	4.2dB equalizer boost gain.	
			0100	5.2dB equalizer boost gain. **Power-up default when EQS = high**.	
			0101	6.2dB equalizer boost gain.	
			0110	7dB equalizer boost gain.	
			0111	8.2dB equalizer boost gain.	
			1000	9.4dB equalizer boost gain.	
			1001	10.7dB equalizer boost gain. **Power-up default when EQS = low**.	
			1010	11.7dB equalizer boost gain.	
			1011	13dB equalizer boost gain.	
			11XX	Do not use.	
0x06	D7	DISSTAG	0	Enable staggered outputs.	0
			1	Disable staggered outputs.	
	D6	AUTORST	0	Do not automatically reset error registers and outputs.	0
			1	Automatically reset error registers and outputs.	
	D5	DISINT	0	Enable interrupt transmission to serializer.	0
			1	Disable interrupt transmission to serializer.	
	D4	INT	0	INT input = low (read only).	0 (read only)
			1	INT input = high (read only).	
	D3	GPIO1OUT	0	Output low to GPIO1.	1
			1	Output high to GPIO1.	
	D2	GPIO1	0	GPIO1 is low.	1 (read only)
			1	GPIO1 is high.	
	D1	GPIO0OUT	0	Output low to GPIO0.	1
			1	Output high to GPIO0.	
	D0	GPIO0	0	GPIO0 is low.	1 (read only)
			1	GPIO0 is high.	

Table 12. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x07	D[7:0]	—	01010100	Reserved.	01010100
0x08	D[7:0]	—	00110000	Reserved.	00110000
0x09	D[7:0]	—	11001000	Reserved.	11001000
0x0A	D[7:0]	—	00010010	Reserved.	00010010
0x0B	D[7:0]	—	00100000	Reserved.	00100000
0x0C	D[7:0]	ERRTHR	XXXXXXXX	Error threshold for decoding errors. $\overline{ERR}$ = low when DECERR > ERRTHR.	00000000
0x0D	D[7:0]	DECERR	XXXXXXXX	Decoding error counter. This counter remains zero while the device is in PRBS test mode.	00000000 (read only)
0x0E	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter.	00000000 (read only)
0x12	D7	MCLKSRC	0	MCLK derived from PCLKOUT (see Table 4).	0
			1	MCLK derived from internal oscillator.	
	D[6:0]	MCLKDIV	0000000	MCLK disabled.	0000000
			XXXXXXX	MCLK divider.	
0x1E	D[7:0]	ID	00000010	Device identifier (MAX9270 = 0x02).	00000010 (read only)
0x1F	D[7:4]	—	0000	Reserved.	0000 (read only)
	D[3:0]	REVISION	XXXX	Device revision.	(read only)

Typical Application Circuit



Gigabit Multimedia Deserializer with Spread Spectrum and Full-Duplex Control Channel

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+2	21-0135	90-0046

Gigabit Multimedia Deserializer with Spread -Spectrum and Full-Duplex Control Channel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	1/11	Added Patent Pending to *Features*	1