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August 2001
Revised August 2001

FIN1531
5V LVDS 4-Bit High Speed Differential Driver

General Description

This quad driver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates 5V TTL/CMOS signal levels to LVDS levels with a typical differential output swing of 350 mV which provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1531 can be paired with its companion receiver, the FIN1532, or with any other Fairchild LVDS receiver.

Features

- Greater than 400Mbs data rate
- 5V power supply operation
- 400ps max differential pulse skew
- 2.0ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and PECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1531M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1531MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

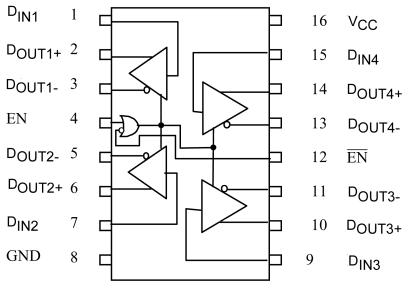
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Function Table

Input			Outputs	
EN	$\overline{EN}$	D_{IN}	D_{OUT+}	D_{OUT-}
H	X	H	H	L
H	X	L	L	H
H	X	OPEN	L	H
X	L	H	H	L
X	L	L	L	H
X	L	OPEN	L	H
L	H	X	Z	Z

H = HIGH Logic Level L = LOW Logic Level
X = Don't Care Z = High Impedance

Connection Diagram



Pin Descriptions

Pin Name	Description
D_{IN1}, D_{IN2}, D_{IN3}, D_{IN4}	5V TTL/CMOS Data Input
D_{OUT1+}, D_{OUT2}+, D_{OUT3+}, D_{OUT4+}	Non-inverting LVDS Output
D_{OUT1-}, D_{OUT2-}, D_{OUT3-}, D_{OUT4-}	Inverting LVDS Output
EN	Driver Enable Pin
$\overline{EN}$	Inverting Driver Enable Pin
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +6V
DC Input Voltage (V_{IN})	−0.5V to +6V
DC Output Voltage (V_{OUT})	−0.5V to +6V
Driver Short Circuit Current (I_{OSD})	Continuous
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 8000V
ESD (Machine Model)	≥ 400V

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0 to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{OD}	Output Differential Voltage	RL = 100Ω, driver enabled, See Figure 1	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OFF}	Power Off Output Current	V_{CC} = 0V, V_{OUT} = 5.5V			50	µA
I_{OS}	Short Circuit Output Current	V_{OUT} = 0V, Driver Enabled			−6	mA
		V_{OD} = 0V, Driver Enabled			±6	
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-OFF Input Current	V_{CC} = 0V, V_{IN} = 5.5V			50	µA
I_{OZ}	Disabled Output Leakage Current	EN = 0.8V, $\overline{EN}$ = 2.0V, V_{OUT} = 0V or 7V			±20	µA
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5	−0.8		V
I_{CC}	Power Supply Current	No Load, V_{IN} = 0V or V_{CC}, Driver Enabled		3.3	6	mA
		R_L = 100Ω, Driver Disabled		3.4	6	
		R_L = 100Ω, V_{IN} = 0V or V_{CC}, Driver Enabled		18	26	
C_{IN}	Input Capacitance			7		pF
C_{OUT}	Output Capacitance			4.5		pF

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 5.0V.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLHD}	Differential Propagation Delay LOW-to-HIGH	R_L = 100 Ω, C_L = 10 pF, See Figure 2 and Figure 3 (Note 7)	0.5	1.4	2.0	ns
t_{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.5	1.4	2.0	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.6	0.8	1.2	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.6	0.8	1.2	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$				0.4	ns
$t_{SK(LH)}$, $t_{SK(HL)}$	Channel-to-Channel Skew (Note 4)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				1.0	ns
f_{MAX}	Maximum Frequency(Note 6)		200	250		ns
t_{ZHD}	LVTTL Output Enable Time from Z to HIGH	R_L = 100Ω, C_L = 10 pF, See Figure 4 and Figure 5 (Note 7)			5.0	ns
t_{ZLD}	LVTTL Output Enable Time from Z to LOW				5.0	ns
t_{HZD}	LVTTL Output Disable Time from HIGH to Z				5.0	ns
t_{LZD}	LVTTL Output Disable Time from LOW to Z				5.0	ns

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 5V.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: f_{MAX} Criteria: Input $t_R = t_F$ < 1 ns, 0V to 3V, 50% Duty Cycle; Output V_{OD} > 250 mV, 45% to 55% Duty Cycle; all output channels switching in phase.

Note 7: Test Circuits in Figure 2 and Figure 4 are simplified representations of test fixture and DUT loading.

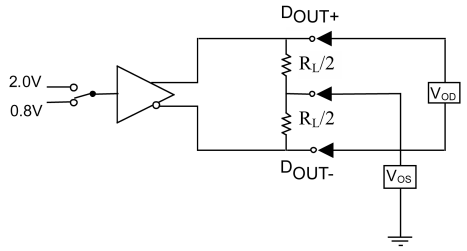
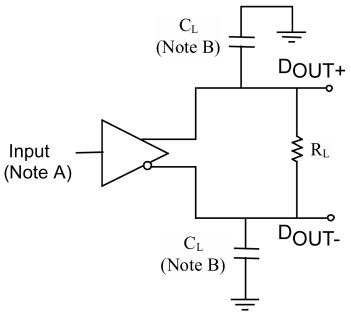


FIGURE 1. Differential Driver DC Test Circuit



Note A: Input pulses have frequency = 10 MHz, t_R or t_F = 1 ns

Note B: C_L includes all probe and jig capacitances

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

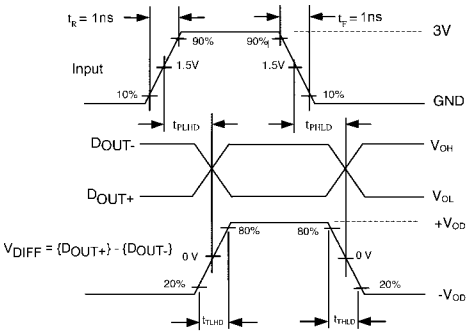
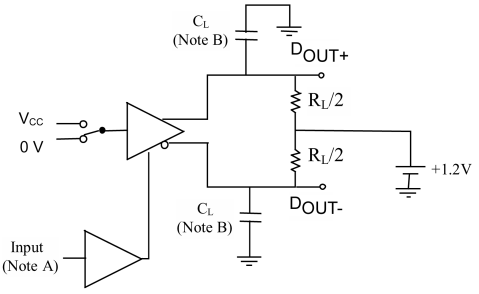


FIGURE 3. AC Waveforms



Note A: Input pulses have the following characteristics:
Frequency = 10 MHz, t_R or t_F = 1 ns

Note B: C_L includes probes and jig capacitance

FIGURE 4. Differential Driver Enable and Disable Test Circuit

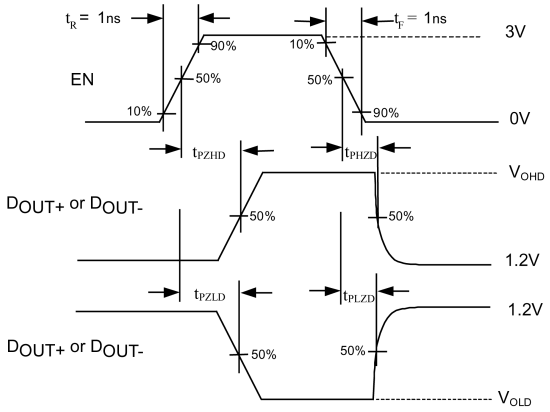
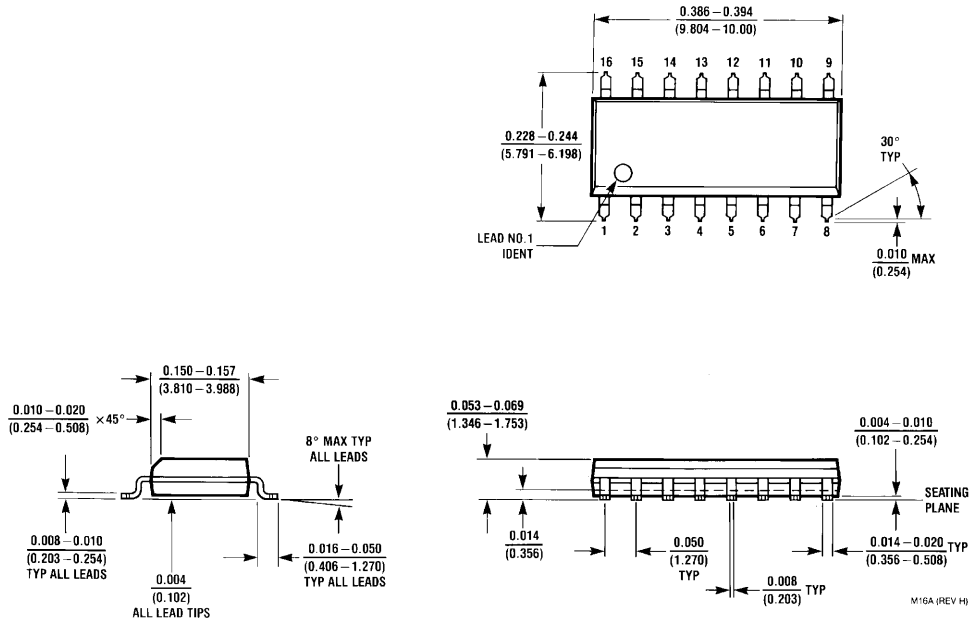


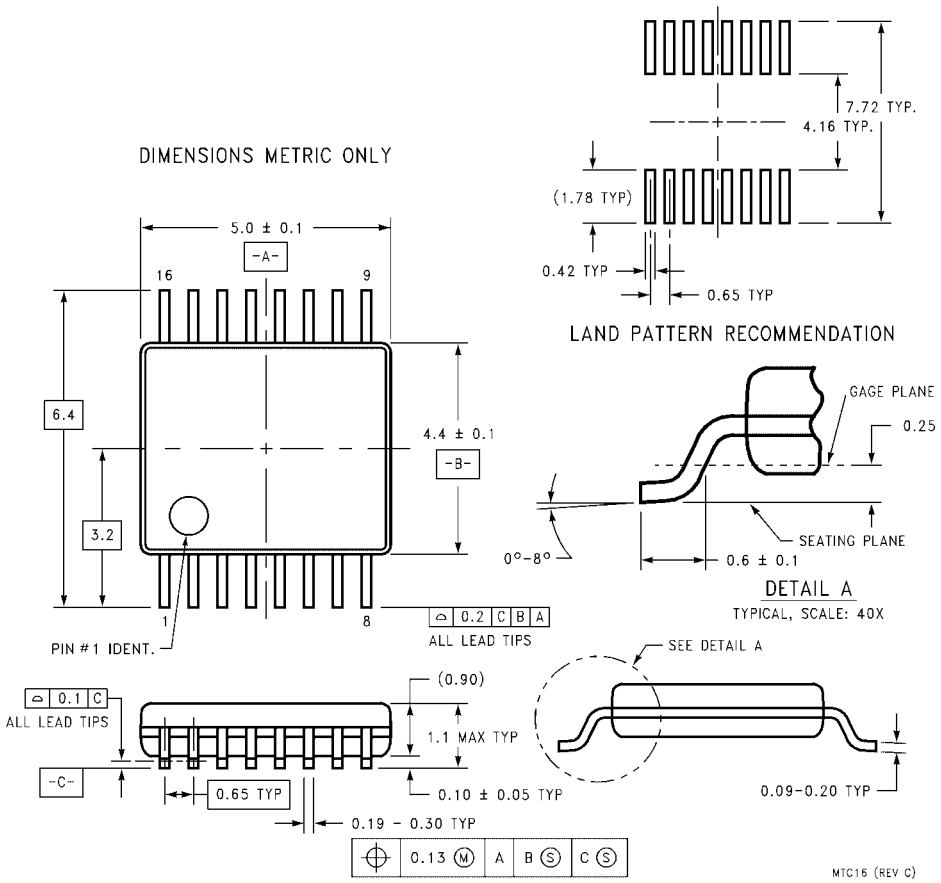
FIGURE 5. Enable and Disable AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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