REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 11-01-19	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, CMOS, ±% V/ +5V , 4 Ω, SINGLE SPDT SWITCH, MONOLITHIC SILICON
	SIZE A **CODE IDENT. NO.** 16236	**DWG NO.** **V62/11608**
	REV	**PAGE** 1 **OF** 12

AMSC N/A

5962-V029-11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS, ±5 V/ +5 V, 4 Ω, single SPDT switch microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer,s PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11608	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG619-EP	CMOS, ±5 V/ +5 V, 4 Ω, single SPDT switch

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MO-178	Small outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage referenced :
- V_{DD} to V_{SS} ..... 13.0 V
- V_{DD} to GND ..... -0.3 V to +6.5 V
- V_{SS} to GND ..... +0.3 V to -6.5 V

Analog input 2/ ..... V_{SS} – 0.3 V to V_{DD} + 0.3 V
Digital input 2/ ..... -0.3 V to V_{DD} + 0.3 V or 30 mA (which ever occurs first)
Peak current, S or D ..... 100 MA (pulsed at 1 ms, 10% duty cycle mzximum)
Continuous current, S or D ..... 50 mA
Ambient operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... 150°C
Thermal impedance:
- θ_{JA} ..... 229°C /W
- θ_{JC} ..... 91.99°C /W

Lead soldering:
- Reflow, peak temperature ..... 260(+0/-5)°C
- Time at peak temperature ..... 20 sec to 40 sec

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th St., Suite 240-S, Arlington, VA 22201-2107 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Overvoltage at IN, S or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 On Resistance. The On resistance shall be as shown in figure 5.

3.5.6 Off Leakage. The Off leakage shall be as shown in figure 6.

3.5.7 On Leakage . The On leakage shall be as shown in figure 7.

3.5.8 Switching times. The switching times shall be as shown in figure 8.

3.5.9 Break before making time delay. The break before making time delay shall be as shown in figure 9.

3.5.10 Charge injection. The charge injection shall be as shown in figure 10.

3.5.11 Off isolation. The Off isolation shall be as shown in figure 11.

3.5.12 Channel to channel crosstalk. The channel to channel crosstalk shall be as shown in figure 12.

3.5.13 Bandwidth. The bandwidth shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits				Unit
			T_A = 25°C		-55°C ≤ T_A ≤ +125°C		
			Min	Max	Min	Max	
DUAL SUPPLY							
Analog switch							
Analog signal range		V_{DD} = +4.5 V, V_{SS} = -4.5 V			V_{SS}	V_{DD}	V
On resistance	R_{ON}	V_S = ±4.5 V, I_{DS} = -10 mA See figure 5		6.5		10	Ω
R_{ON} Match between channels	ΔR_{ON}	V_S = ±4.5 V, I_{DS} = -10 mA		1.1		1.45	
On resistance flatness	$R_{FLAT (ON))}$	V_S = ±3.3 V, I_{DS} = -10 mA		1.35		1.6	
Leakage currents (V_{DD} = +5.5 V, V_{SS} = -5.5 V)							
Source off leakage,	I_S(Off)	V_S = ±4.5 V, V_D = ±4.5 V, See figure 6		±0.25		±3	nA
Channel On leakage,	I_D, I_S (On)	V_S = V_D = ±4.5 V, See figure 7		±0.25		±25	
Digital inputs							
Input high voltage	V_{INH}				2.4		V
Input low voltage	V_{INL}					0.8	
Input current,	I_{NL} or I_{NH}	V_{IN} = V_{INL} or V_{INH}	0.05 TYP			±0.1	µA
Digital input capacitance	C_{IN}		2 TYP				pF
Dynamic characteristic 3/							
t_{ON}		R_L = 300 Ω, C_L = 35 pF,		220		390	ns
t_{OFF}		V_S = 3.3 V, See figure 8		75		135	
Break before make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3.3 V, See figure 9	70 TYP		10		
Charge injection		V_S -= 0 V, R_S = 0 Ω, C_L = 1 nF, See figure 10	6 TYP				pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 11	- 67 TYP				dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 12	- 67 TYP				
Bandwidth -3 dB		R_L = 50 Ω, C_L = 5 pF, See figure 13	190 TYP				MHz
C_S (Off)		f = 1 MHz	25 TYP				pF
C_D, C_S (On)			95 TYP				
Power requirements (V_{DD} = +5.5 V, V_{SS} = -5.5 V)							
I_{DD}		Digital inputs = 0 V or 5.5 V	0.001 TYP			1.0	µA
I_{SS}			0.001 TYP			1.0	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics Continued. 1/

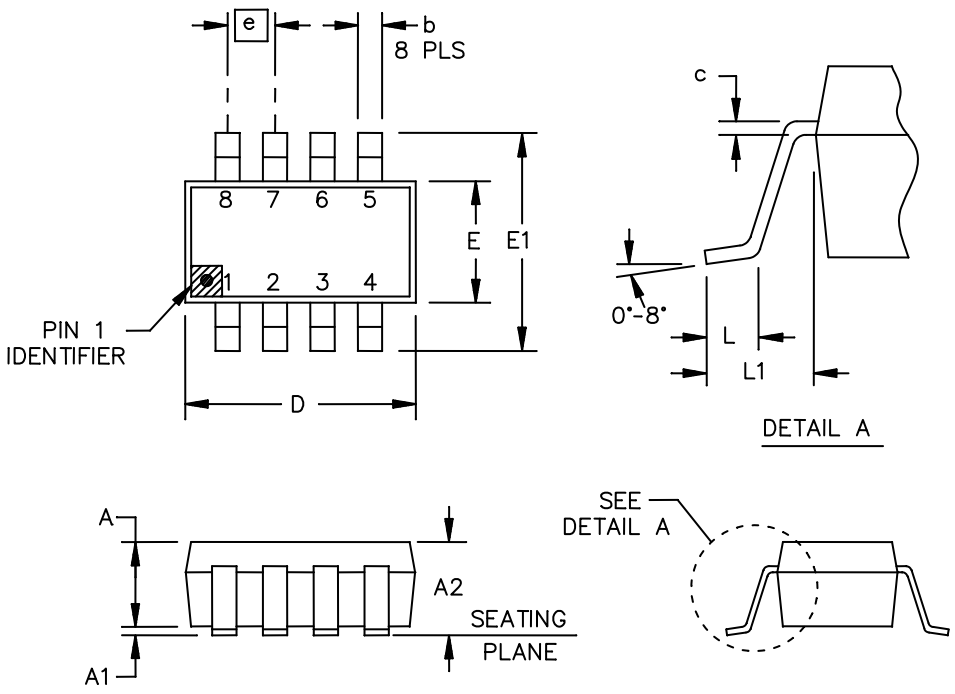
Test	Symbol	Test conditions 2/ unless otherwise specified	Limits				Unit
			T_A = 25°C		-55°C ≤ T_A ≤ +125°C		
			Min	Max	Min	Max	
SINGLE SUPPLY							
Analog switch							
Analog signal range		V_{DD} = +4.5 V, V_{SS} = -0 V			0	V_{DD}	V
On resistance	R_{ON}	V_S = 0 V to 4.5 V, I_{DS} = -10 mA See figure 5		10		14	Ω
R_{ON} Match between channels	ΔR_{ON}	V_S = 0 V to 4.5 V, I_{DS} = -10 mA		1.1		1.4	
On resistance flatness	$R_{FLAT (ON))}$	V_S =1.5 V to 3.3 V, I_{DS} = -10 mA	0.5 TYP			1.4	
Leakage currents (V_{DD} = +5.5 V)							
Source off leakage,	I_S(Off)	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, See figure 6		±0.25		±3	nA
Channel On leakage,	I_D, I_S (On)	V_S = V_D = ±4.5 V, See figure 7		±0.25		±25	
Digital inputs							
Input high voltage	V_{INH}				2.4		V
Input low voltage	V_{INL}					0.8	
Input current,	I_{NL} or I_{NH}	V_{IN} = V_{INL} or V_{INH}	0.05 TYP			±0.1	µA
Digital input capacitance	C_{IN}		2 TYP				pF
Dynamic characteristic 3/							
t_{ON}		R_L = 300 Ω, C_L = 35 pF,		120		215	ns
t_{OFF}		V_S = 3.3 V, See figure 8		75		105	
Break before make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3.3 V, See figure 9	40 TYP		10		
Charge injection		V_S -= 0 V, R_S = 0 Ω, C_L = 1 nF, See figure 10	110 TYP				pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 11	- 67 TYP				dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 12	- 67 TYP				
Bandwidth -3 dB		R_L = 50 Ω, C_L = 5 pF, See figure 13	190 TYP				MHz
C_S (Off)		f = 1 MHz	25 TYP				pF
C_D, C_S (On)			95 TYP				
Power requirements (V_{DD} = +5.5 V)							
I_{DD}		Digital inputs = 0 V or 5.5 V	0.001 TYP			1.0	µA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 5 V ±10%, V_{SS} = 0 V, GND = 0 V, -55°C ≤ T_A ≤ 125°C, unless otherwise noted.

3/ Guaranteed by design, not subject to production test.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.90	1.30	E	1.50	1.70
A1	0.05	0.15	E1	2.60	3.00
A2	0.95	1.45	e	0.65 BSC	
b	0.22	0.38	L	0.30	0.60
c	0.08	0.22	L1	0.60 BSC	
D	2.80	3.00			

FIGURE 1. Case outline.

Case outline X

Pin No.	Mnemonic	Description
1	D	Drain terminal. Can be an input or output
2	S1	Source terminal. Can be an input or output
3	GND	Ground (0 V) reference.
4	V_{DD}	Most positive power supply
5	NC	No connect. Not internal connected.
6	IN	Logic control input
7	V_{SS}	Most negative power supply. This pin is only used in dual supply applications and should be tied to ground in single supply applications.
8	S2	Source terminal. can be an input or output

FIGURE 2. Terminal connections.

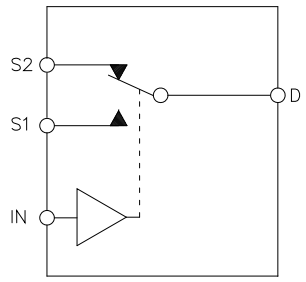


FIGURE 3. Functional block diagram.

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

FIGURE 4. Truth table.

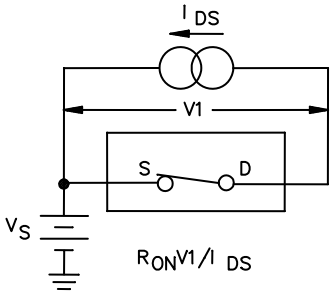


FIGURE 5. ON Resistance.

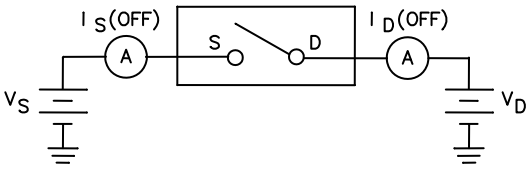


FIGURE 6. OFF leakage.

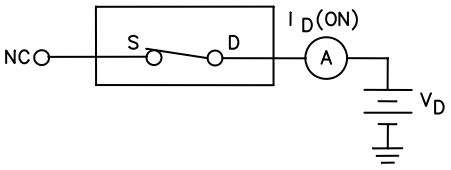


FIGURE 7. ON Leakage.

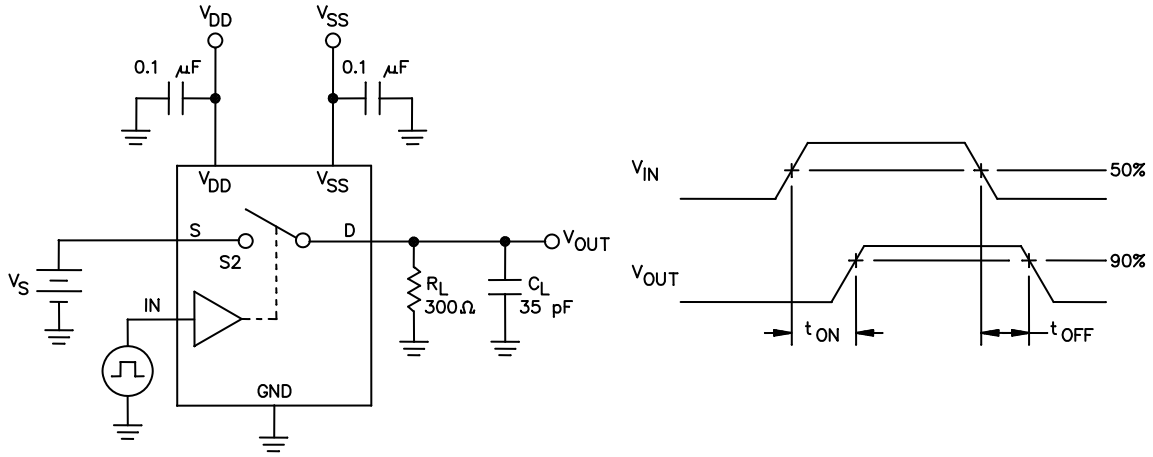


FIGURE 8. Switching times.

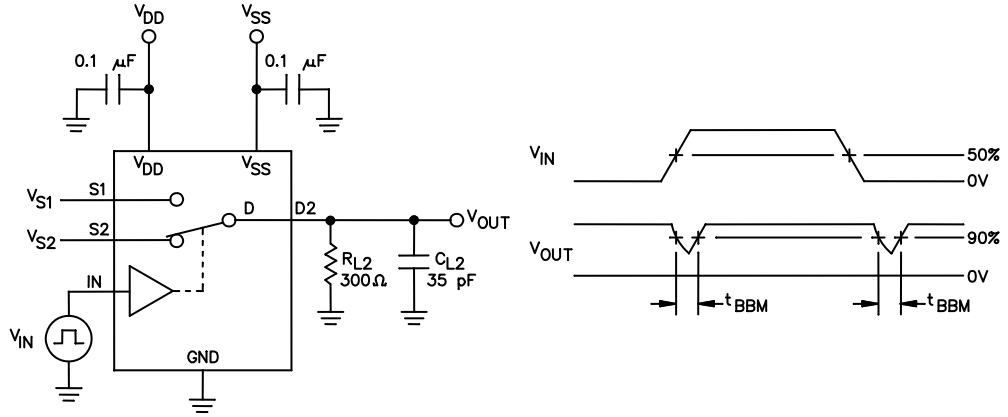


FIGURE 9. Break before make time delay.

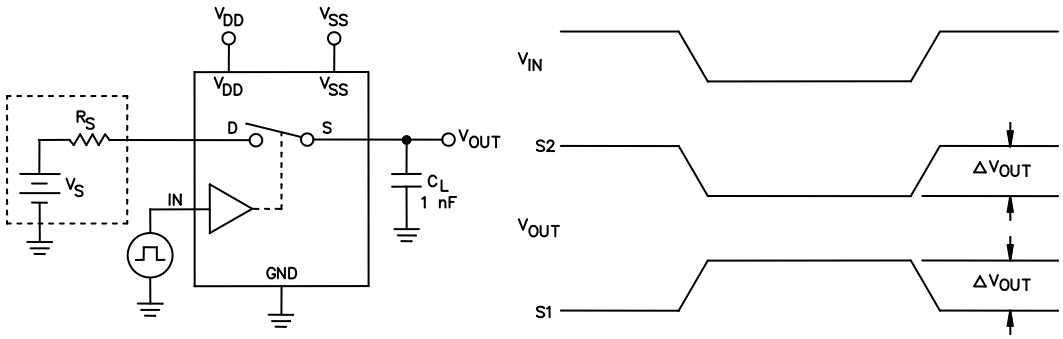
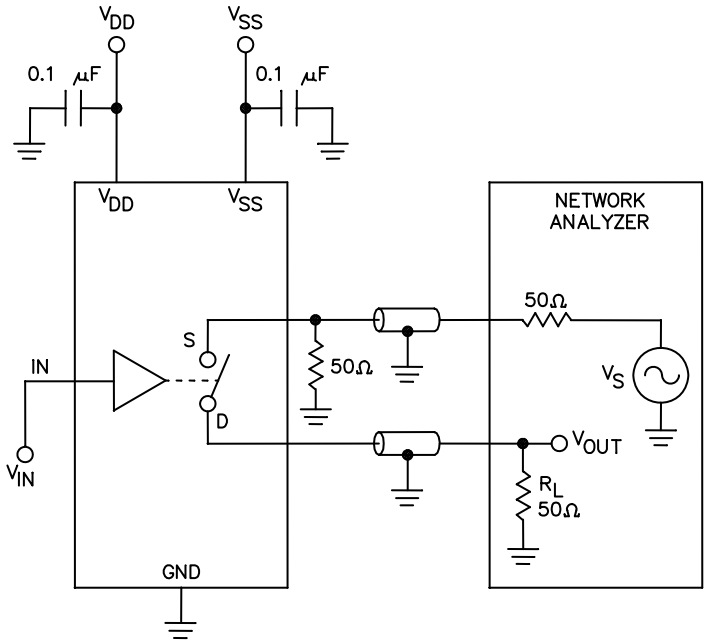
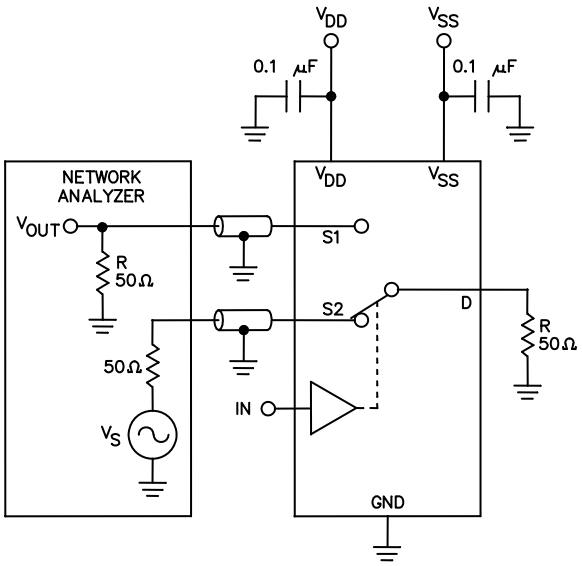


FIGURE 10. Charge injection.



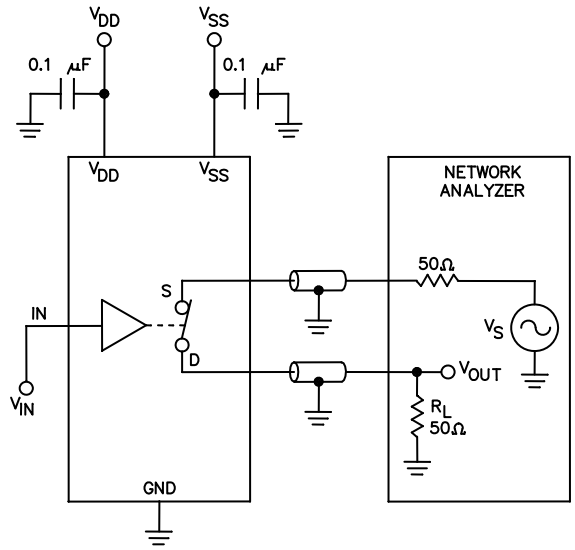
$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

FIGURE 11. Off isolation.



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

FIGURE 12. Channel to channel crosstalk.



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT} \text{ WITH SWITCH}}{V_S \text{ WITHOUT SWITCH}}$$

FIGURE 13. Bandwidth.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11608-01XE	24355	ADG619SRJZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605