DATASHEET

40V Precision Instrumentation Amplifier with Differential ADC Driver

ISL28617

The ISL28617 is a high performance, differential input, differential output instrumentation amplifier designed for precision analog-to-digital applications. It can operate over a supply range of 8V (±4V) to 40V (±20V) and features a differential input voltage range up to ±34V. The output stage has rail-to-rail output drive capability optimized for differential ADC driver applications. Its versatility and small package makes it suitable for a variety of general purpose applications. Additional features not found in other instrumentation amplifiers enable high levels of DC precision and excellent AC performance.

The gain of the ISL28617 can be programmed from 0.1 to 10,000 via two external resistors, R_{IN} and R_{FB}. The gain accuracy is determined by the matching of R_{IN} and R_{FB}. The gain resistors have Kelvin sensing, which removes gain error due to PC trace resistance. The input and output stages have individual power supply pins, which enable input signals riding on a high common mode voltage to be level shifted to a low voltage device, such as an A/D converter. The rail-to-rail output stage can be powered from the same supplies as the ADC, which preserves the ADC maximum input dynamic range and eliminates ADC input overdrive.

Related Literature

- AN1753, "ISL28617VYXXEV1Z User's Guide" Evaluation board with bulk metal foil resistors for high precision.
- AN1748, "ISL28617SMXXEV1Z User's Guide" Evaluation board with standard resistors for low cost, medium precision.

Features

- Rail-to-rail differential output ADC driver
- High voltage interface to low voltage circuits
- Wide operating voltage range . . . . . ±4V to ±20V
- Low input offset 30µV
- Excellent CMRR and PSRR 120dB
- Closed loop -3dB BW . . .0.3MHz (A_V = 1k) to 5MHz (A_V = 0.1)
- Operating temperature range. . . . . -40°C to +125°C
- Package. . . . . 24 Ld TSSOP

Applications

- Precision test and measurement
- High voltage industrial process control
- Signal conditioning amplifier for remote powered sensors
- Weigh scales
- ECG and biomedical sense amplifiers

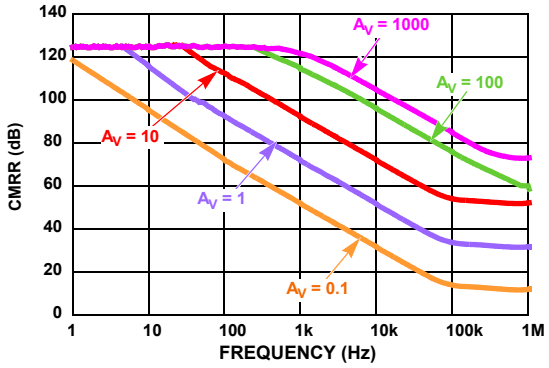


FIGURE 1. CMRR R_F = 121k

FULL BRIDGE STRAIN GAUGE AMPLIFIER AND DIFFERENTIAL ADC DRIVER

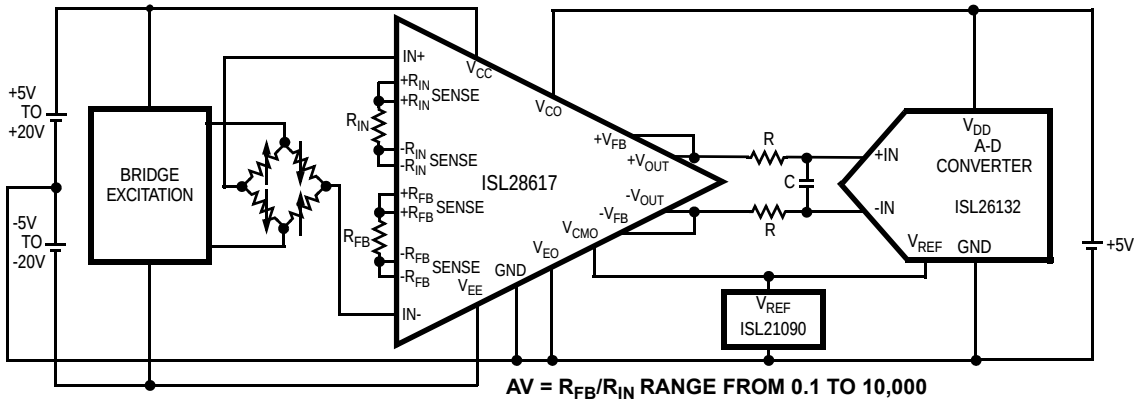
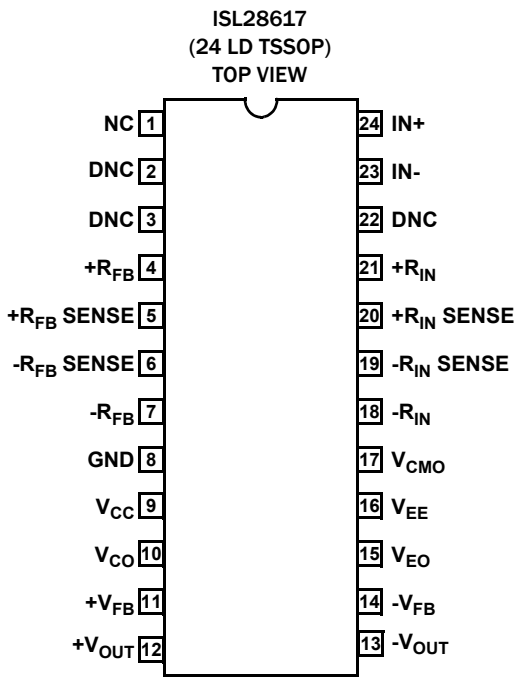


FIGURE 2. BASIC APPLICATION CIRCUIT



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
NC	1	No Internal Connection
DNC	2, 3, 22	For internal use; Do Not Connect.
$+R_{FB}$	4	Feedback Resistor, R_{FB}+ pin
$+R_{FB}$ SENSE	5	$+R_{FB}$, Positive Sense pin connects to the resistor R_{FB}+ terminal to form the R_{FB}+ Kelvin connection.
$-R_{FB}$ SENSE	6	$-R_{FB}$, Negative Sense pin connects to the resistor R_{FB}- terminal to form the R_{FB}- Kelvin connection.
$-R_{FB}$	7	Feedback Resistor, Negative Terminal.
GND	8	Ground Pin is capacitively coupled to the internal ESD circuit and should be connected to power supply common or signal GND.
V_{CC}	9	Positive Supply for Input Stage and Feedback Amp.
V_{CO}	10	Positive Supply for Output Stage.
$+V_{FB}$	11	Positive Output Feedback
$+V_{OUT}$	12	Positive Output
$-V_{OUT}$	13	Negative Output
$-V_{FB}$	14	Negative Output Feedback
V_{EO}	15	Negative Supply for Output Stage.
V_{EE}	16	Negative Supply for Input Stage and Feedback Amp.
V_{CMO}	17	Output Common Mode Reference input.
$-R_{IN}$	18	Input Resistor, Negative Terminal.
$-R_{IN}$ SENSE	19	$-R_{IN}$, Negative Sense pin connects to the resistor R_{IN}- terminal to form the R_{IN}- Kelvin connection.
$+R_{IN}$ SENSE	20	$+R_{IN}$, Positive Sense pin connects to the resistor R_{IN}+ terminal to form the R_{IN}+ Kelvin connection.
$+R_{IN}$	21	Input Resistor, Positive Terminal.
IN-	23	Negative Input
IN+	24	Positive Input

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28617FVZ	28617 FVZ	-40 to +125	24 Ld TSSOP	M24.173

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28617. For more information on MSL please see tech brief TB363.

Simplified Block Diagram

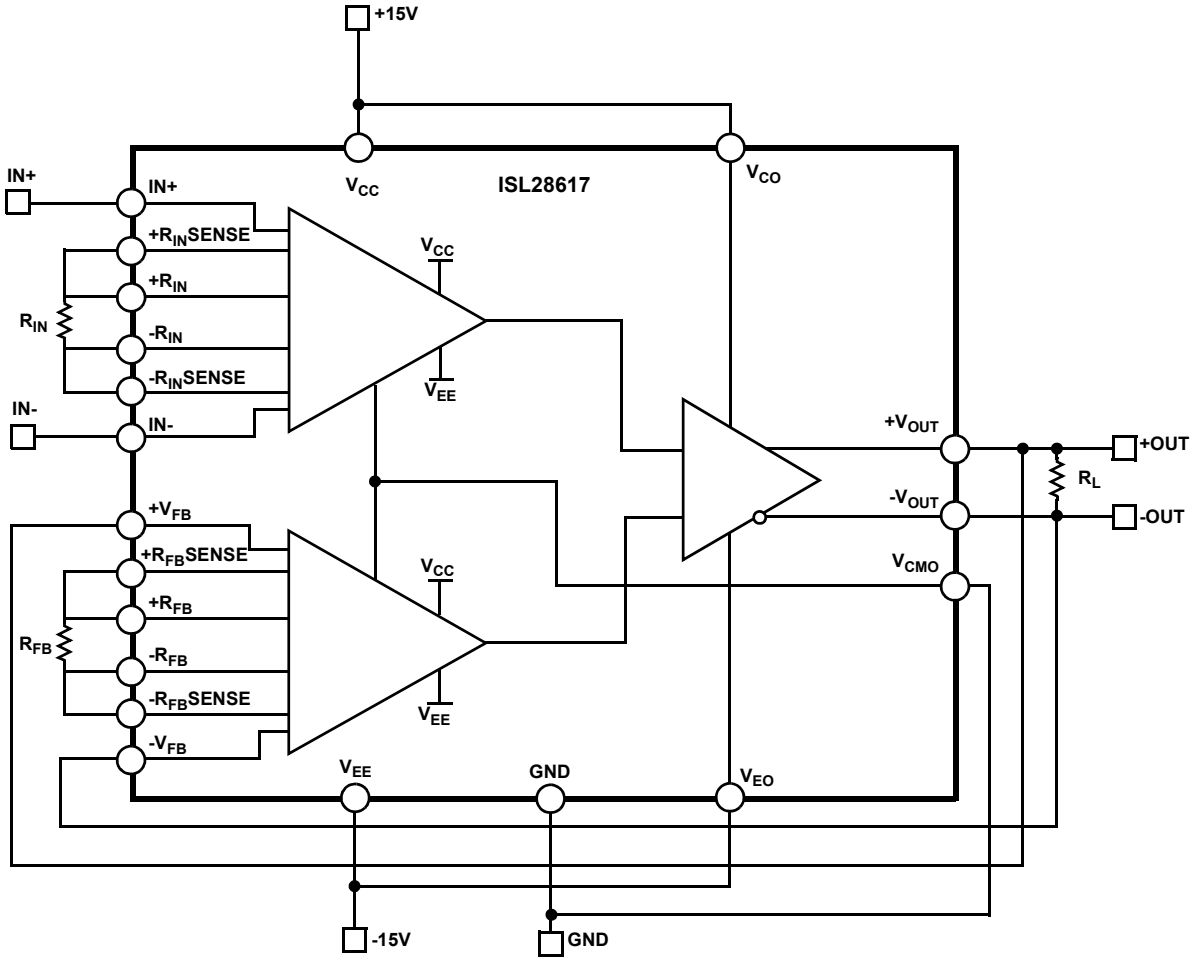


FIGURE 3. SIMPLIFIED BLOCK DIAGRAM

Absolute Maximum Ratings

Maximum Supply Voltage (V_{CC} to V_{EE} or GND) 42V
Maximum Supply Voltage (V_{CO} to V_{EO} or GND) 42V
Maximum Voltage (V_{CO} to V_{CC}) . . . . . +0.5V, -40V
Maximum Voltage (V_{EO} to V-) . . . . . -0.5V, +40V
Maximum Differential Input Current . . . . . ±10mA
Max/Min Input Current for Input Voltage >V_{CC} or <V_{EE} . . . . . ±10mA
Maximum Input Current (±R_{IN}, ±R_{FB}, ±R_{IN}SENSE, ±R_{FB}SENSE) . . . . ±5mA
Maximum Differential Input Voltage 40V
Min/Max Input Voltage . . . . . (V_{EE} - 0.5V) to (V_{CC} + 0.5V)
Output Short-circuit Duration (1 Output at a Time). . . . . Continuous
ESD Rating
Human Body Model 4kV
Machine Model 200V
Charged Device Model 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld TSSOP (Notes 4, 5)	74	28

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +125°C
V_{CC}, V_{EE} Operating Voltage Range . . . . . ±4V to ±20V
V_{CO}, V_{EO} Operating Voltage Range . . . . . ±1.5V to ±20V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

$V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$, $R_{FB} = R_{IN} = 30.1k\Omega$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT DC SPECIFICATIONS						
V_{CMIR}IN	IN+, IN- Common Mode Input Voltage Range		**V_{EE} +3V**		**V_{CC} -3V**	V
V_{OS}IN	Input Offset Voltage		-100	±30	100	µV
			-275		**275**	µV
TCV_{OS}IN	Input Offset Voltage Temperature Coefficient		**-2.75**	±0.3	**2.75**	µV/°C
I_BIN	Input Bias Current		-1	±0.2	1	nA
			-1.3		**1.3**	nA
I_{OS}IN	Input Offset Current		-0.75	±0.2	0.75	nA
			-1		**1**	nA
I_{RIN}	Input Resistor Drive Current	(Note 7)	87	102	117	µA
R_{IN}CM	Common Mode Input Resistance			80		GΩ
CMRR	Common Mode Rejection Ratio	V_{EE} +3V ≤ V_{CM} ≤ V_{CC} -3V, G = 1	110	120		dB
			107			dB
		V_{EE} +3V ≤ V_{CM} ≤ V_{CC} -3V, G = 100	130	150		dB
			110			dB
FEEDBACK DC SPECIFICATIONS						
V_{CMIR}FB	+FB, -FB Common Mode Input Voltage Range		**V_{EE} + 3V**		**V_{CC} - 3V**	V
V_{OS}FB	Feedback Input Offset Voltage		-1600	±400	1600	µV
			-3000		**3000**	µV
$I_B V_{FB+,-}$	Input Bias Current at V_{FB} ± Inputs			15		nA
OUTPUT DC SPECIFICATIONS						
V_{OL}	Output Voltage Low, V_{OUT} to V_-	V_{CC} = +15V, V_{EE} = -15V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F = 121k\Omega$, I_{OUT} = 1.5mA		150	200	mV
					200	mV

Electrical Specifications $V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$, $R_{FB} = R_{IN} = 30.1k\Omega$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OH}	Output Voltage High, V_+ to V_{OUT}	V_{CC} = +15V, V_{EE} = -15V, V_{CO} = +4V, V_{EO} = -4V $R_{IN} = R_F = 121k\Omega$, I_{OUT} = 1.5mA		150	200	mV
					200	mV
I_{SC}	Output Short-circuit Current	R_L = 0Ω to GND		±45		mA
			-20		**20**	mA
I_{ERR}	Total Internal Offset Error Current (Note 8)		-17	±5	17	nA
			-90		**90**	nA
E_G	Gain Error (Notes 9, 10)	V_{OUT} = -10V to +10V, R_F = 121kΩ		±0.003		%
		G = 1				
		G = 100		±0.004		%
		V_{OUT} = -2.5V to +2.5V, R_F = 30.1kΩ		±0.0005		%
		G = 1				
OUTPUT COMMON MODE SPECIFICATIONS						
V_{CMO}CMIR	Output Common Mode Control Input Voltage Range		**V_{EE} +3V**		**V_{CC} -3V**	V
V_{OS}CM	Output Common Mode Offset Voltage from V_{CMO} Input		-1.3	±0.5	1.3	mV
			-4.75		**4.75**	mV
$I_B V_{CMO}$	Input Bias Current at V_{CMO} Input		-0.6	±0.2	0.6	µA
			-1.75		**1.75**	µA
POWER SUPPLY SPECIFICATIONS						
I_{CC}	Supply Current, V_{CC} to V_{EE}	R_L = OPEN		2.05	2.2	mA
					2.85	mA
I_{CO}	Supply Current, V_{CO} to V_{EO}	R_L = OPEN		2.25	2.6	mA
					2.85	mA
V_{CC} to V_{EE}	Input Supply Voltage	Dual Supply	±4		±20	V
		Single Supply	8		40	V
V_{CO} to V_{EO}	Output Supply Voltage	Dual Supply	±1.5		±20	V
		Single Supply	3		40	V
PSRR V_{CC} to V_{EE}	Power Supply Rejection Ratio	V_{CC} to V_{EE} = ±4V to ±20V				dB
		G = 100	123	130		
			118			dB
PSRR V_{CO} to V_{EO}	Power Supply Rejection Ratio	V_{CO} to V_{EO} = ±4V to ±20V	110	120		dB
			110			dB
AC SPECIFICATIONS						
e_N	Input Noise Voltage Density	f = 1kHz		8.6		nV/√Hz
$e_N$rms	Input rms Noise Voltage	f = 0.1 to 10Hz		85		nVrms
i_N	Input Noise Current Density	f = 1kHz		150		fA/√Hz
i_NIERR	Total Internal Noise Current Density	f = 1kHz		2.6		pA/√Hz
i_NIERR rms	0.1 to 10Hz Total Internal rms Noise Current	f = 0.1 to 10Hz		4		pArms

Electrical Specifications $V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$, $R_{FB} = R_{IN} = 30.1k\Omega$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
-3dB BW	-3dB Bandwidth vs Closed Loop Gain, R_{FB} = 30.1k	$R_{FB} = 30.1k\Omega$; $R_{IN} = 301k\Omega$; G = 0.1		5.5		MHz
		$R_{FB} = 30.1k\Omega$; $R_{IN} = 30.1k\Omega$; G = 1		2.6		MHz
		$R_{FB} = 30.1k\Omega$; $R_{IN} = 3.01k\Omega$; G = 10		2.2		MHz
		$R_{FB} = 30.1k\Omega$; $R_{IN} = 301\Omega$; G = 100		2.0		MHz
		$R_{FB} = 30.1k\Omega$; $R_{IN} = 30.1\Omega$; G = 1000		0.3		MHz
-3dB BW	-3dB Bandwidth vs Closed Loop Gain, R_{FB} = 121k	$R_{FB} = 121k\Omega$; $R_{IN} = 1.21M\Omega$; G = 0.1		5.0		MHz
		$R_{FB} = 121k\Omega$; $R_{IN} = 121k\Omega$; G = 1		1.4		MHz
		$R_{FB} = 121k\Omega$; $R_{IN} = 12.1k\Omega$; G = 10		0.5		MHz
		$R_{FB} = 121k\Omega$; $R_{IN} = 1.21k\Omega$; G = 100		0.45		MHz
		$R_{FB} = 121k\Omega$; $R_{IN} = 121\Omega$; G = 1000		0.4		MHz
SR	Slew Rate			4		V/µs
t_S	Settling Time to 0.01%	$V_{OUT} = \pm 2.4V$, $R_F = 30.1k\Omega$		3		µs
		$V_{OUT} = \pm 9.6V$, $R_F = 121k\Omega$		11		µs

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Compliance to datasheet limits is assured by Design simulation.
8. $V_{OS,OUT} = A_V * V_{OS,IN} + V_{OS,FB} + I_{ERR} * R_{FB}$.
9. Differential Gain(A_V) = R_{FB}/R_{IN}.
10. $\pm V_{OUT}$, clipping ~ $I_{RF} * R_{FB}$.

Typical Performance Curves

$V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

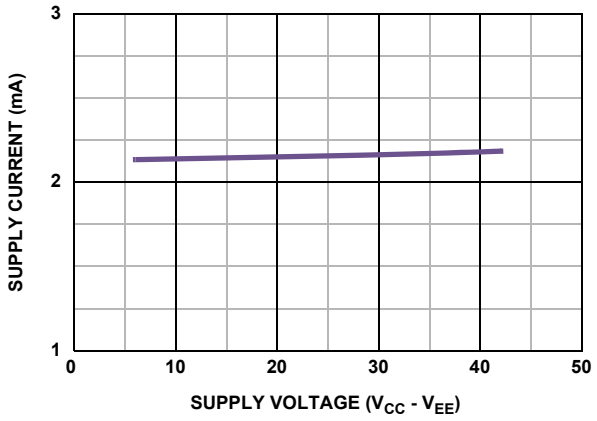


FIGURE 4. I_{CC} vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

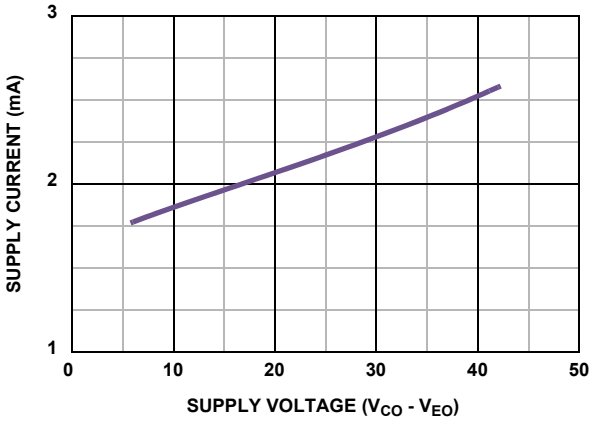


FIGURE 5. I_{CO} vs SUPPLY VOLTAGE (V_{CO} - V_{EO})

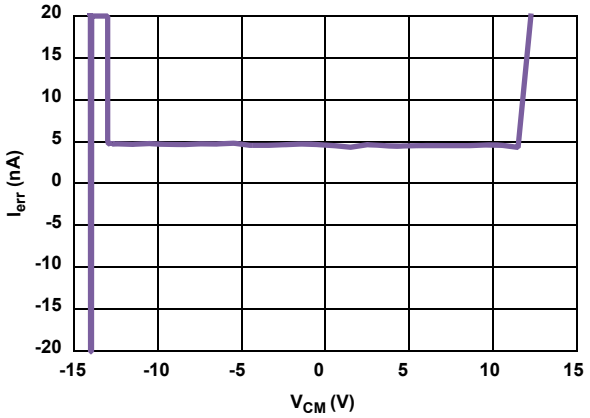


FIGURE 6. I_{ERR} vs INPUT COMMON MODE VOLTAGE

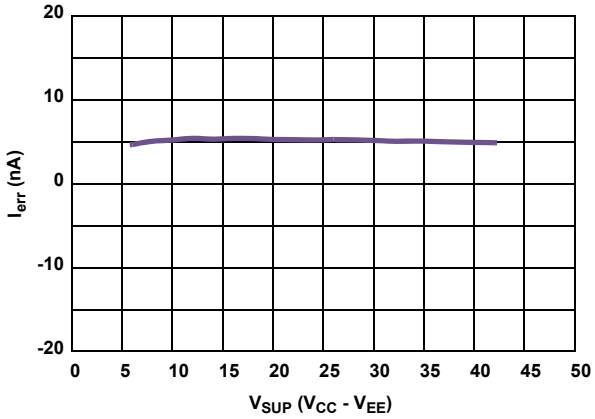


FIGURE 7. I_{ERR} vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

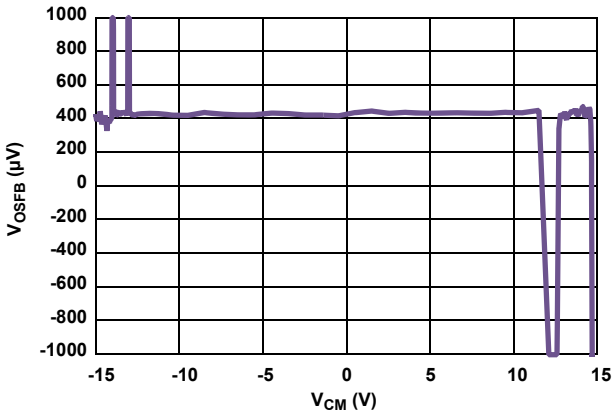


FIGURE 8. V_{OSFB} vs INPUT COMMON MODE VOLTAGE

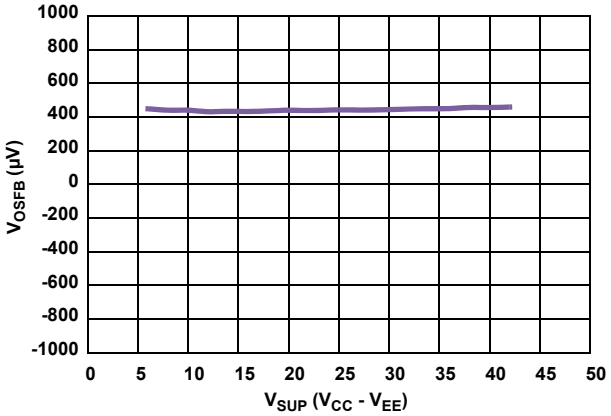


FIGURE 9. V_{OSFB} vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

Typical Performance Curves

$V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

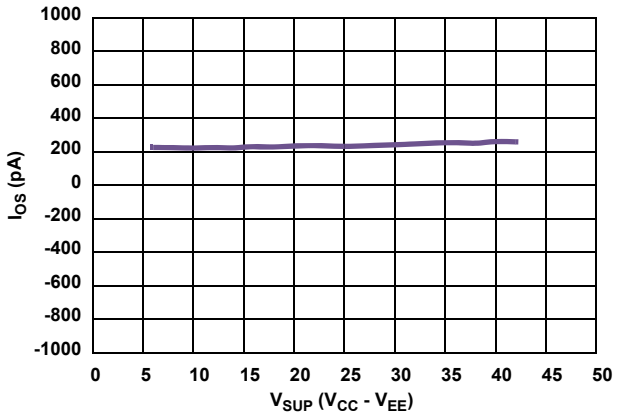


FIGURE 10. I_{OS} vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

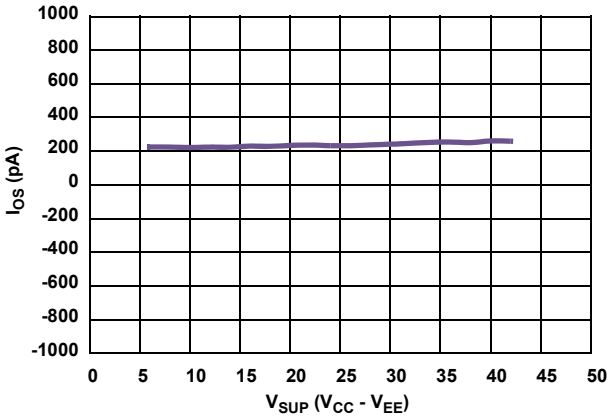


FIGURE 11. I_{OS} vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

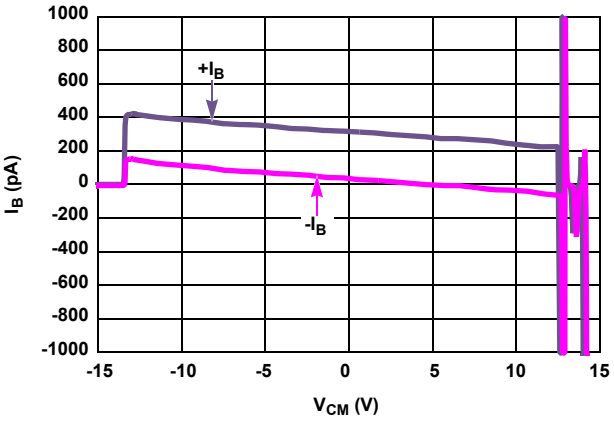


FIGURE 12. I_B vs INPUT COMMON MODE VOLTAGE

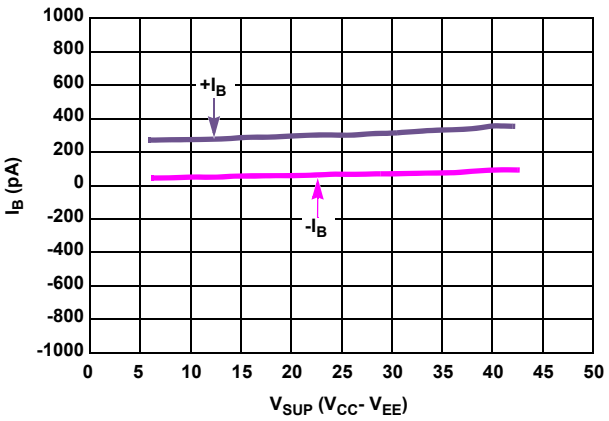


FIGURE 13. I_B vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

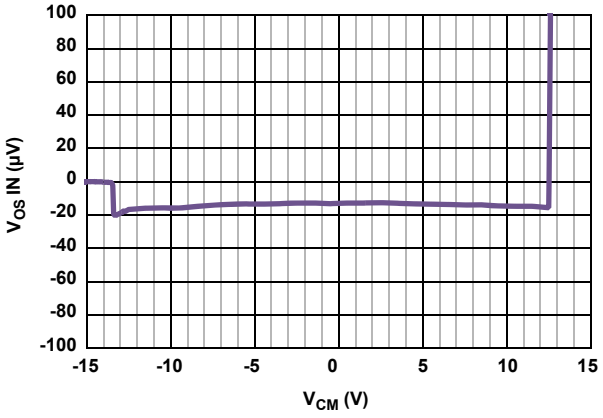


FIGURE 14. V_{OS} IN vs INPUT COMMON MODE VOLTAGE

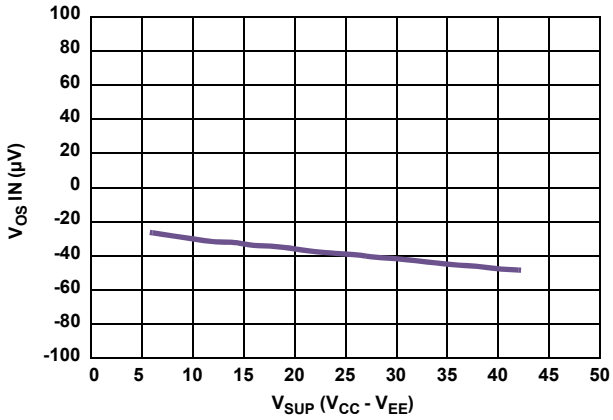


FIGURE 15. V_{OS} IN vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

Typical Performance Curves

$V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

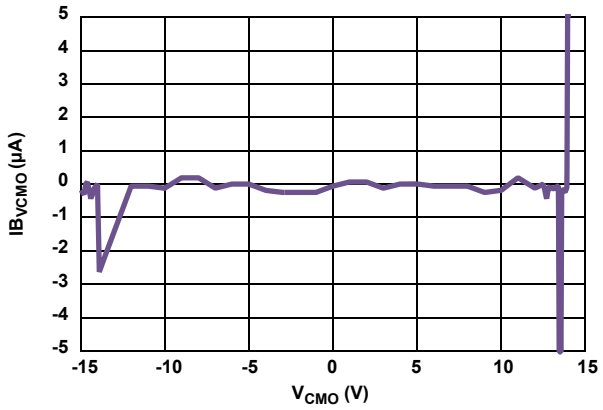


FIGURE 16. IB_{VCMO} vs V_{CMO} INPUT VOLTAGE RANGE

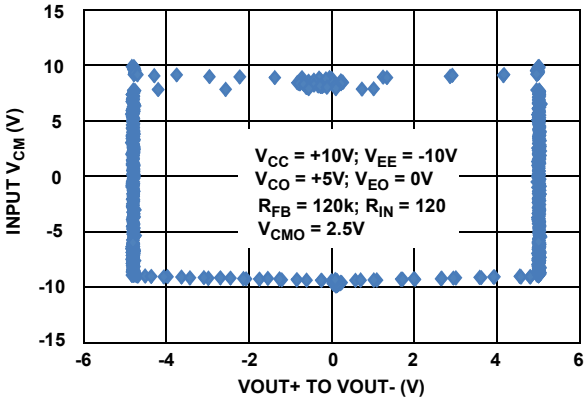


FIGURE 17. COMMON MODE RANGE vs OUTPUT VOLTAGE

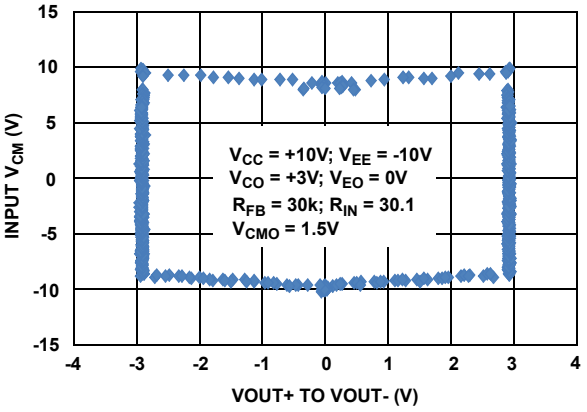


FIGURE 18. COMMON MODE RANGE vs OUTPUT VOLTAGE

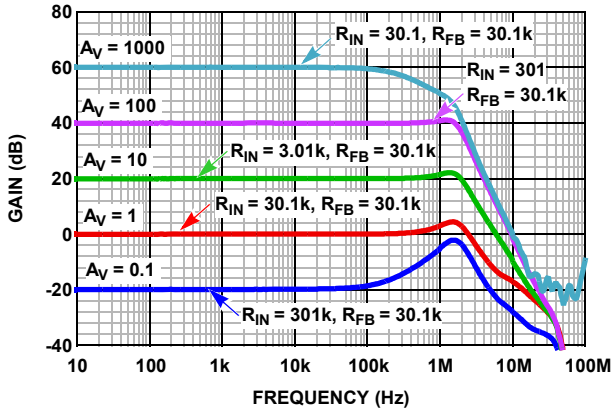


FIGURE 19. CLOSED LOOP GAIN (R_{FB} = 30.1k) vs FREQUENCY

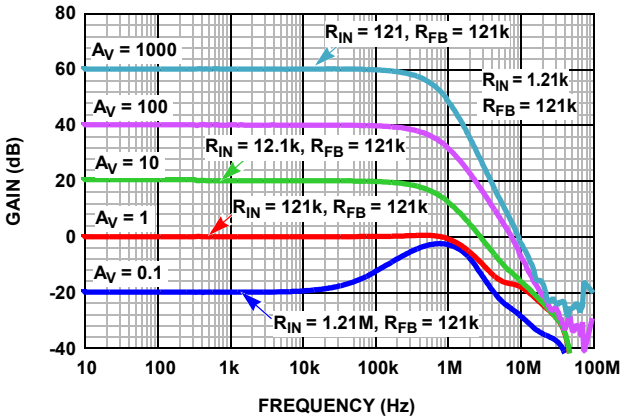


FIGURE 20. CLOSED LOOP GAIN (R_{FB} = 121k) vs FREQUENCY

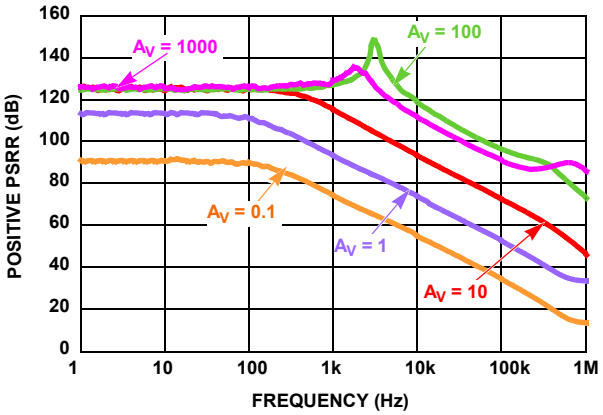


FIGURE 21. POSITIVE PSRR V_{EE} AND V_{CC} (R_F = 30.1k)

Typical Performance Curves

$V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

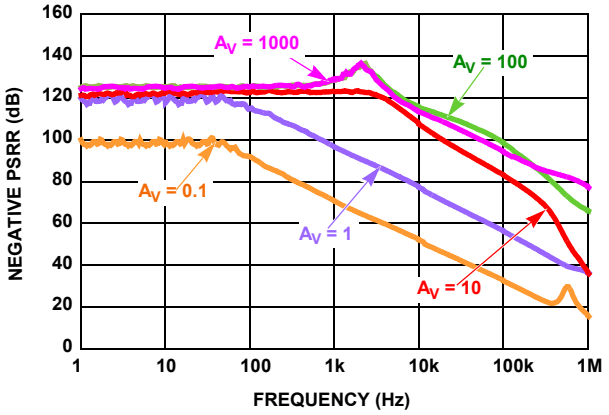


FIGURE 22. NEGATIVE PSRR V_{EE} AND V_{CC} (R_F = 30.1k)

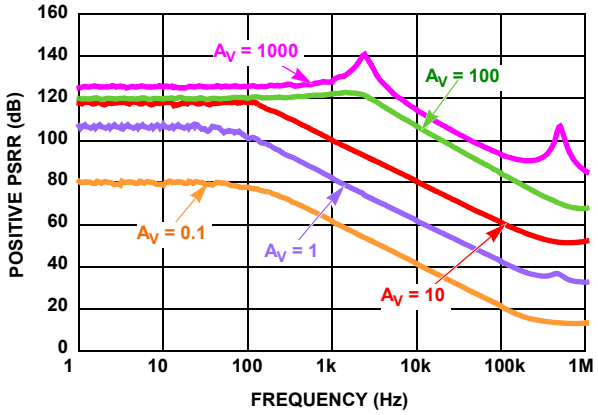


FIGURE 23. POSITIVE PSRR V_{EE} AND V_{CC} (R_F = 121k)

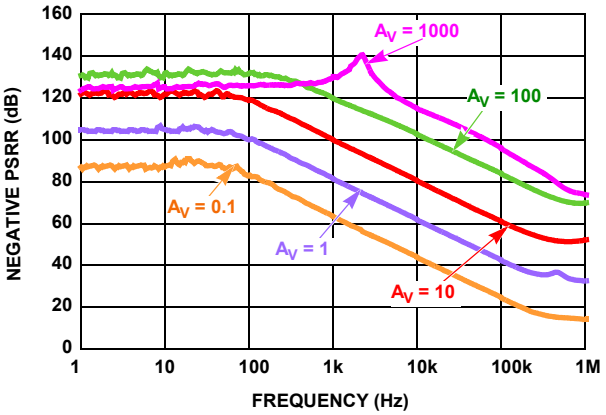


FIGURE 24. NEGATIVE PSRR V_{EE} AND V_{CC} (R_F = 121k)

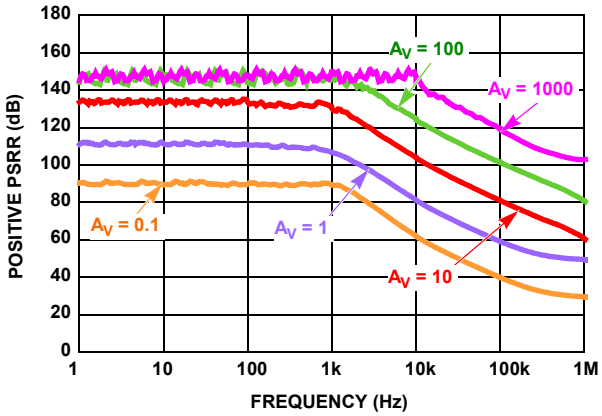


FIGURE 25. POSITIVE PSRR V_{EO} AND V_{CO} (R_F = 30.1k)

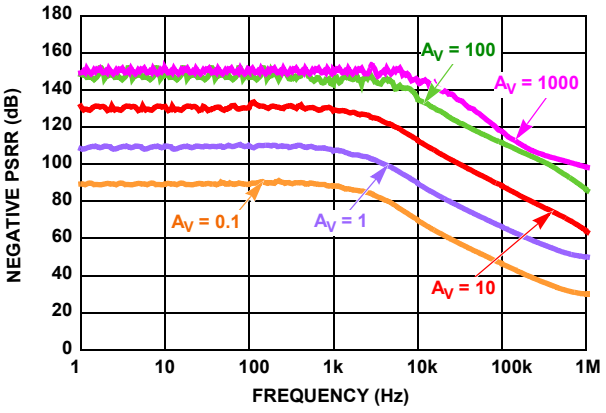


FIGURE 26. NEGATIVE PSRR V_{EO} AND V_{CO} (R_F = 30.1k)

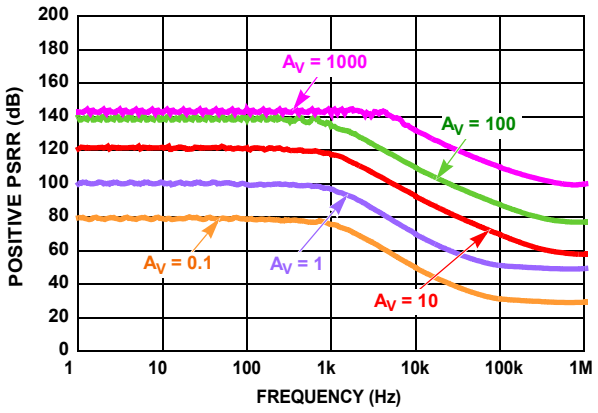


FIGURE 27. POSITIVE PSRR V_{EO} AND V_{CO} (R_F = 121k)

Typical Performance Curves

$V_{CC} = V_{CO} = 15V$, $V_{EE} = V_{EO} = -15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

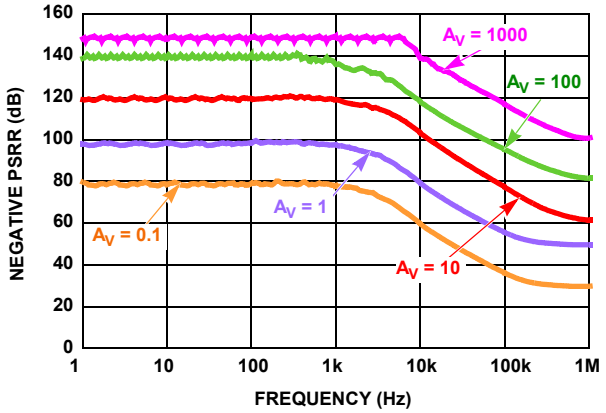


FIGURE 28. NEGATIVE PSRR V_{E0} AND V_{CO} (R_F = 121k)

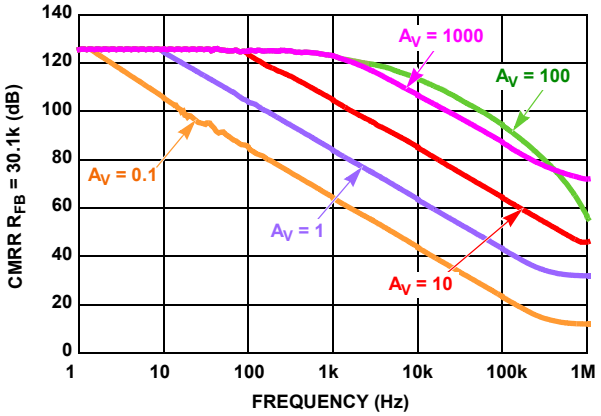


FIGURE 29. CMRR RF = 30.1k

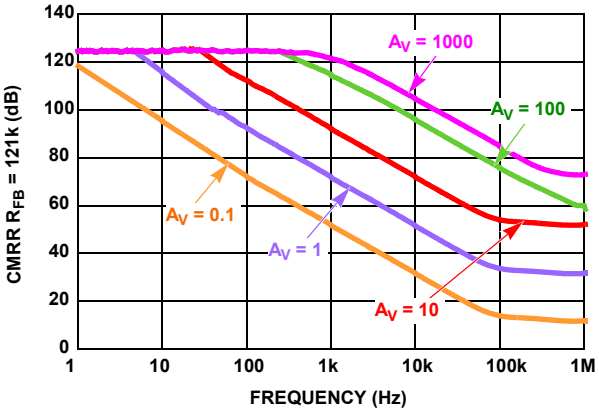


FIGURE 30. CMRR R_F = 121k

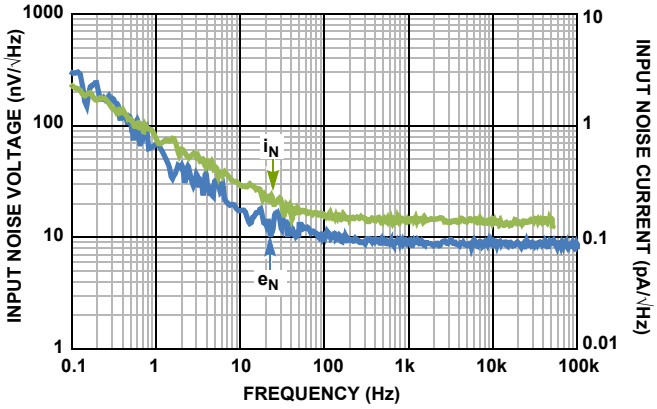


FIGURE 31. INPUT VOLTAGE AND CURRENT NOISE

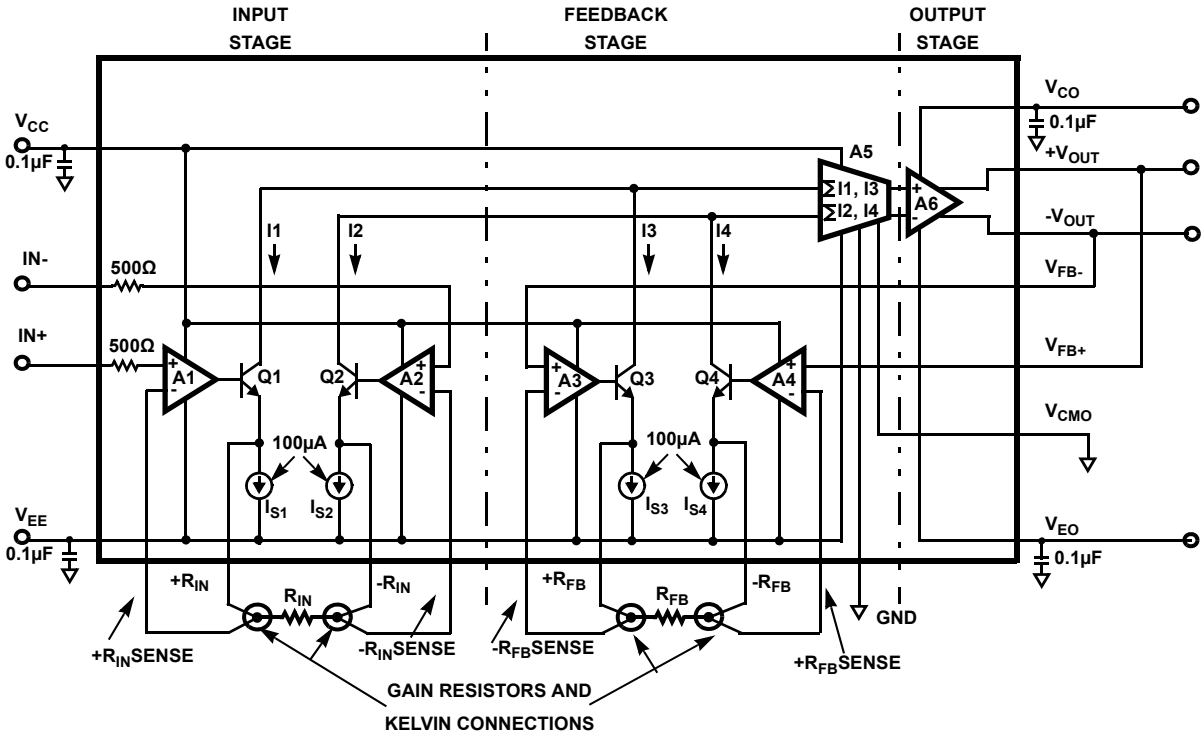


FIGURE 32. ISL28617 FUNCTIONAL BLOCK DIAGRAM

Applications Information

"General Description" section: contains the ISL28617 functional and performance objectives and description of operation.

"Designing with the ISL28617" on page 14 section: contains the application circuit design equations and guidelines for achieving the desired DC and AC performance levels.

"Estimating Amplifier DC and Noise Performance" on page 17 section: provides equations for predicting DC offset voltage and noise of the finished design.

General Description

The ISL28617 Instrumentation Amplifier was developed to accomplish the following:

- Provide a fully differential, rail-to-rail output for optimally driving ADCs.
- Limit the output swing to prevent output overdrive.
- Allow any gain, including attenuation.
- Maximize gain accuracy by removing on-chip component tolerances and external PC board parasitic resistance.
- Enable user control of amplifier precision level with choice of external resistor tolerance.
- Maintain CMRR>100dB and remove CMRR sensitivity to gain resistor tolerance.
- Provide a level shift interface from bipolar analog input signal sources to unipolar and bipolar ADC output terminations.

Functional Description

Figure 32 shows the functional block diagram for the ISL28617.

Input G_M Amplifier

The input stage consists of high performance, wide band amplifiers A1, A2, G_M drive transistors Q1, Q2 and input gain resistor R_{IN}. Current drive for Q1 and Q2 emitters are provided by matched pair of 100µA current sinks. A unity gain buffer from each input (IN+, IN-) to the terminals of the input resistor, R_{IN}, is formed by the connection of the Kelvin resistor sense pins and drive pins to the terminals of the input resistor, as shown in Figure 32. In this configuration, the voltage across the input resistor R_{IN} is equal to the input differential voltage across IN+ and IN-.

The input G_M stage operates by creating a current difference in the collector currents Q1 and Q2 in response to the voltage difference between the IN+ and IN- pins. When the input voltage applied to the IN+ and IN- pins is zero, the voltage across the terminals of the gain resistor R_{IN}, is also zero. Since there is no current flow through the gain resistor, transistors Q1 and Q2 collector currents I_1 and I_2 are equal.

A change in the input differential voltage causes an equivalent voltage drop across the input gain resistor R_{IN} and the resulting current flow through R_{IN}, causes an imbalance in Q1 and Q2 collector currents I_1 and I_2, given by Equations 1 and 2:

$$I_1 = 100\mu A + (V_{IN+} - V_{IN-})/R_{IN} \quad \text{(EQ. 1)}$$

$$I_2 = 100\mu A - (V_{IN+} - V_{IN-})/R_{IN} \quad \text{(EQ. 2)}$$

Feedback G_M Amplifier

The feedback amplifiers A3 and A4 form a differential transconductance amplifier identical to the input stage. The input terminals (V_{FB+}, V_{FB-}) connect to the ISL28617 differential output terminals ($+V_{OUT}$, $-V_{OUT}$), so that the output voltage also appears across the feedback gain resistor R_{FB}.

Operation is the same as the input G_M stage and the differential currents I_3 and I_4 are given by Equations 3 and 4:

$$I_3 = 100\mu A - \{(+V_{OUT}) - (-V_{OUT})\}/R_{FB} \quad \text{(EQ. 3)}$$

$$I_4 = 100\mu A + \{(+V_{OUT}) - (-V_{OUT})\}/R_{FB} \quad \text{(EQ. 4)}$$

Error Amplifier A5, Output Amplifier A6 (Figure 32)

Amplifiers A5 and A6 act together to form a high gain, differential I/O trans impedance amplifier. Differential current amplifier A5 sums the differential currents ($I_1 + I_3$ and $I_2 + I_4$) from the input and feedback G_M amplifiers. From that summation, a differential error voltage is sent to A6, which generates the rail-to-rail differential output drive to the $+V_{OUT}$ and $-V_{OUT}$ pins.

The external connection of the output pins to the feedback amplifier closes a servo loop where a change in the differential input voltage is converted into differential current imbalances at I_1 and I_2 (Equations 1 and 2) at the summing node inputs to A5. Current I_1 sums with current I_3 from the feedback stage and I_2 sums with I_4. A5 senses the difference between current pairs I_1, I_3 and I_2, I_4. A difference voltage is generated, amplified and fed back to the feedback amplifier, which creates correction currents at I_3 and I_4 to match the currents at I_1 and I_2 (Equations 3 and 4).

Therefore, at equilibrium:

$$I_1 = I_3 \text{ and } I_2 = I_4 \quad \text{(EQ. 5)}$$

Combining Equations 1 and 3, (and their complements I_2 and I_4) and solving for V_{OUT} as a function of V_{IN}, R_{IN} and R_{FB}, yields Equation 6:

$$V_{OUT} = (V_{IN} \times R_{FB})/R_{IN} \quad \text{(EQ. 6)}$$

Where $V_{OUT} = (+V_{OUT}) - (-V_{OUT})$ and $V_{IN} = IN+ - IN-$

Equation 6 can be rearranged to form the gain, see Equation 7:

$$\text{Gain} = V_{OUT}/V_{IN} = R_{FB}/R_{IN} \quad \text{(EQ. 7)}$$

Which is general form of the gain equation for the ISL28617.

Designing with the ISL28617

To complete a working design, the following procedure is recommended:

1. Define the output voltage swing
2. Set the feedback resistor value, R_{FB}
3. Set the input gain resistor value, R_{IN}
4. Set the V_{CO}, V_{EO} power supply voltages
5. Set the V_{CC} and V_{EE} supply voltages

The gain of the instrumentation amplifier is set by the resistor ratio R_{FB}/R_{IN} (Equation 7) and the maximum output swing is set by the absolute value of the feedback resistor R_{FB} (Equation 8). V_{CO} and V_{EO} supply power to the rail-to-rail output stage and define the maximum output voltage swing at the $\pm V_{OUT}$ differential output pins. Power supply pins V_{CC} and V_{EE} power the feedback amplifiers, which require an additional ±3V beyond the V_{CO} and V_{EO} voltages to maintain linear operation of the feedback G_M stage.

Setting the Feedback Gain Resistor R_{FB} (Figures 32, 33)

Resistor R_{FB} defines the maximum differential voltage at output terminals $+V_{OUT}$ to $-V_{OUT}$. External resistor R_{FB} and the differential 100µA current sources define the maximum dynamic range of the feedback stage, which defines the maximum differential output swing of the output stage. Overload circuitry allows >100µA to flow through R_{FB} to maintain feedback, but linearity is degraded. Therefore, it is a good practice to keep the maximum linear dynamic range to within ±80% of the maximum I*R across the resistor.

$$V_{OUT}DIFF = \pm 80_{\mu A} \times R_{FB} \quad \text{(EQ. 8)}$$

In cases where large pulse overshoot is expected, the maximum current in Equation 8 could be reduced to 50% for additional margin (see "AC Performance Considerations" on page 16). The penalty for increasing the feedback resistor value is higher DC offset voltage and noise.

Output voltages that exceed the maximum dynamic range of the feedback amplifier can degrade phase margin and cause instability. The plot in Figure 33 shows the maximum differential output voltage swing vs resistor value for R_{FB} and R_{IN} using the 80% and 50% current source levels.

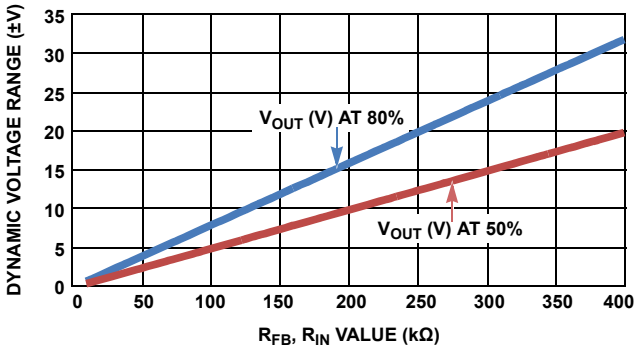


FIGURE 33. R_{FB}, R_{IN} vs DYNAMIC RANGE

Setting the Input Gain Resistor R_{IN} (Figures 32, 33)

The input gain resistor R_{IN} is scaled to the feedback resistor according to the gain shown by Equation 9:

$$R_{IN} = R_{FB}/Gain \quad \text{(EQ. 9)}$$

The input G_M stage uses the same differential current source arrangement as the feedback stage. Therefore, the amount of overdrive margin (50%, 80%) included in the calculation for R_{FB} is also included in the calculation for R_{IN}.

Input Stage Overdrive Considerations (Figure 34)

There are a few cases where the input stage can be overdriven, which must be considered in the application. An input signal that exceeds the maximum dynamic range of the gain resistor R_{IN}, calculated previously, can cause the ESD diodes to conduct. When this occurs, a low impedance path from the inputs to the input gain resistor R_{IN} will result in signal distortion.

High-speed input signals that remain within the maximum dynamic range of the input stage can cause distortion if the input slew rate exceeds the input stage slew rate (~4V/µs). When the input slews at a faster rate than the G_M stage can follow, the voltage difference appears across the input ESD diodes from each input and resistor R_{IN}. When the voltage difference is large enough to cause the diodes to conduct, the input terminals are shunted to R_{IN} through the 500Ω input protection resistors, causing distortion during the rise and fall times of the transient pulse. The distortion will last until the resistor voltage catches up to the input voltage.

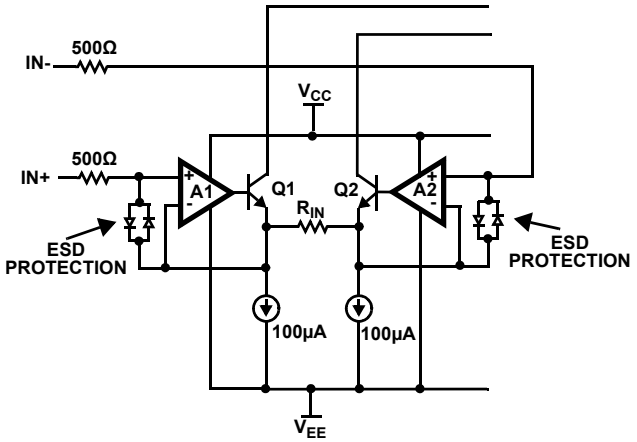


FIGURE 34. INPUT STAGE ESD PROTECTION DIODES

Setting the Power Supply Voltages

The ISL28617 power supplies are partitioned so that the input stage and feedback stages are powered from a separate pair of supply pins (V_{CC}, V_{EE}) than the differential output stage (V_{CO}, V_{EO}). This partitioning provides the user with the ability to adapt the ISL28617 to a wide variety of input signal power sources that would not be possible if the supplies were strapped together internally ($V_{CC} = V_{CO}$ and $V_{EE} = V_{EO}$). However, powering the input and output supplies from unequal supplies has restrictions that are described in the next section.

Powering the Input and Feedback Stages (V_{CC}, V_{EE})

The input pins IN+, IN- cannot swing rail-to-rail, but have a maximum input voltage range given by Equation 10:

$$V_{EE} + 3V \leq (V_{CMIR}IN + V_{IN}) \leq V_{CC} - 3V \quad \text{(EQ. 10)}$$

Where V_{IN} = maximum differential voltage IN+ to IN-

This requires the sum of the common mode input voltage and the differential input voltage to remain within 3V of either the V_{CC} or V_{EE} rail, otherwise distortion will result.

The feedback pins V_{FB}+ and V_{FB}- have the same input common mode voltage constraint as the input pins IN+ and IN-. The maximum input voltage range of the feedback pins is given by Equation 11:

$$V_{EE} + 3V \leq V_{CMIR}FB \leq V_{CC} - 3V \quad \text{(EQ. 11)}$$

Where $V_{CMIR}FB = (+V_{OUT} - -V_{OUT}) + V_{CMO}$

To maintain stability, it is critical to respect the ±3V requirement in Equation 11.

Powering the Rail-to-rail Output Stage (V_{CO}, V_{EO})

The output stage (A6) is of rail-to-rail design and is powered by the V_{CO} and V_{EO} pins. The differential output pins $+V_{OUT}$ and $-V_{OUT}$ connect to the V_{FB}+ and V_{FB}- pins to close the output feedback loop. The feedback stage is powered from V_{CC} and V_{EE} pins. The V_{FB}+ and V_{FB}- have a common mode input range 3V below the V_{CC} rail and 3V above the and V_{EE} rail. If the output voltage exceeds the feedback common mode input voltage, loop instability will result. Therefore, the voltages at the $\pm V_{OUT}$ pins should always be 3V away from either rail, as shown in Equation 12:

$$V_{EE} + 3V \leq V_{OUT} \leq V_{CC} - 3V \quad \text{(EQ. 12)}$$

Where $V_{OUT} = |+V_{OUT}|$ or $|-V_{OUT}|$

Rail-to-rail Differential ADC Driver

The differential output stage of ISL28617 is designed to drive the differential input stage of an ADC. In this configuration, the V_{CO} and V_{EO} power supply pins connect directly to the ADC power supply pins. This output swing arrangement is ideal for driving rail-to-rail ADC drive without the possibility of overdriving the ADC input.

The output stage is capable of rail-to-rail operation when V_{CO} and V_{EO} are powered from a single supply or from split supplies. It has a single supply voltage range (V_{CO}) from 3V to 15V (with V_{EO} at GND) and a ±1.5V to ±15V split supply voltage range. Under all power supply conditions, V_{CC} must be greater than V_{CO} by 3V and V_{EE} must be less than V_{EO} by 3V to maintain the rail-to-rail output drive capability.

The V_{CMO} pin is an input to a very low bias current terminal and sets the output common mode reference voltage when driving a differential input ADC, such that the output would have a ± input signal span centered around an external DC reference voltage applied to the V_{CMO} pin.

Power Supply Voltages by Application

The ISL28617 can be adapted to a wide variety of instrumentation amplifier applications where the signal source is powered from supply voltages that are different from the supply voltages powering downstream circuits. The following examples are included as a guide to the proper connection and voltages applied to the supply pins V_{CC}, V_{EE}, V_{CO} and V_{EO}.

There are a common set of requirements across all power applications:

1. A common ground connection from the input supplies, (V_{CC}, V_{EE}) to the output supplies (V_{CO}, V_{EO}) is required for all powering options.
2. The signal input pins IN+ and IN- cannot float and must have a DC return path to ground.
3. The input and output supplies cannot both be operated in single supply mode due to the 3V feedback amplifier common mode headroom requirement in Equation 11.

The following are typical power examples:

EXAMPLE 1: BIPOLAR INPUT TO SINGLE SUPPLY OUTPUT

The ISL28617 is configured as a 5V ADC driver in a high-gain sensor bridge amplifier powered from a ±10V excitation source. The sensor signal output is at a much lower voltage level. In this application, the ISL28617 must extract the low-level bipolar sensor signal and shift the level to the 0V to +5V differential rail-to-rail signal needed by the ADC. The following powering option is recommended:

- V_{CC} = +10V, V_{EE} = -10V
- V_{CO} = +5V, V_{EO} = GND
- V_{CMO} = +2.5V
- V_{CC} and V_{EE} power supply common connects to GND

EXAMPLE 2: HIGH VOLTAGE BIPOLAR I/O BUFFER

The ISL28617 is configured as a high impedance buffer instrumentation amplifier in a ±15V industrial sensor application. In this application, the ISL28617 must extract and amplify the high impedance sensor signal and send it downstream to a differential ADC operating from ±15V supplies. The following powering options are recommended:

1. Input and output supplies are strapped to the same supplies and rail-to-rail input to the ADC is not required.
   - V_{CC} = V_{CO} = +15V
   - V_{EE} = V_{EO} = -15V
   - V_{CMO} = GND
   - V_{CC}, V_{EE} power supply common connects to GND and V_{OUT} = ±12V
2. ±15V Rail-to-rail output is required, then:
   - V_{CC} = +18V, V_{EE} = -18V
   - V_{CO} = +15V, V_{EO} = -15V
   - V_{CMO} = GND
   - V_{CC} and V_{EE} power supply common connects to GND

The V_{CO} and V_{EO} power supply pins connect to the ADC (±15V) power supply pins. Rail-to-rail output swing requires that $V_{CC} = V_{CO}$ +3V and $V_{EE} = V_{EO}$ -3V, or ±18V.

EXAMPLE 3: GAINS LESS THAN 1

The ISL28617 is configured to a gain of 0.2V/V driving a rail-to-rail 3V ADC. In this application, the maximum input dynamic range is ±15V.

- V_{CC} = +18V, V_{EE} = -18V
- V_{CO} = +3V, V_{EO} = GND
- V_{CMO} = +1.5V
- V_{CC}, V_{EE} power supply common connects to GND

In this attenuator configuration, the input signal range is ±15V, which requires an additional ±3V of input overhead from the input supplies. Thus, V_{CC} and V_{EE} = ±18V.

AC Performance Considerations

The ISL28617 closed loop frequency response is formed by the feedback G_M amplifier and gain resistor R_{FB} and has the characteristics of a current feedback amplifier. Therefore, the -3dB gain does not significantly decrease at high gains as is the case with the constant gain-bandwidth response of the classic voltage feedback amplifier.

There are four behaviors of current feedback amplifiers that must be considered:

- Frequency response increases with decreasing values of R_{FB}. A comparison of the G = 100, -3db response (Figures 19, 20) R_{FB} at 30.1kΩ vs 121kΩ shows almost a 4x decrease from 2MHz to 0.5MHz.
- Gain peaking tends to increase with decreasing values of R_{FB}.
- Wide band applications at gains less than 1 (Figures 19, 20) can have high gain peaking resulting in high levels of overshoot with pulsed input signals.
- Parasitic capacitance at the feedback resistor terminals ($+R_{FB}$, $-R_{FB}$) and the Kelvin sense terminals ($+R_{FB}$SENSE, $-R_{FB}$SENSE) will result in increasing levels of peaking and transient response overshoot.

To minimize peaking external PC parasitic capacitance should be minimized as much as possible. The ISL28617 is designed to be stable with PC board parasitic capacitance up to 20pF and feedback resistor values down to 30.1kΩ. At gains less than 1, the maximum parasitic capacitance may have to be limited further to avoid additional compensation.

Uncorrected gain peaking and high overshoot in the feedback stage can cause loss of feedback loop stability if the transient causes the feedback voltage to exceed the common mode input range of the feedback amplifier or the maximum linear range of the feedback resistor R_{FB}. Corrective actions include increasing the size of the feedback resistor (see Figure 33) and rescaling the input gain resistor R_{IN}, or adding input frequency compensation described in the next section.

The penalty of increasing the R_{FB} (and R_{IN} rescaling) is increased noise, so this is generally not the corrective action of choice.

AC Compensation Techniques

The input compensation with a low pass filter (Figure 35) can be an effective way to block high frequency signals from the differential amplifier inputs. It does not change the gain peaking behavior of the feedback loop, but it does block signals from creating overdrive instability. This method is useful after other corrective measures have been implemented and when there is little control over the input signal frequency content.

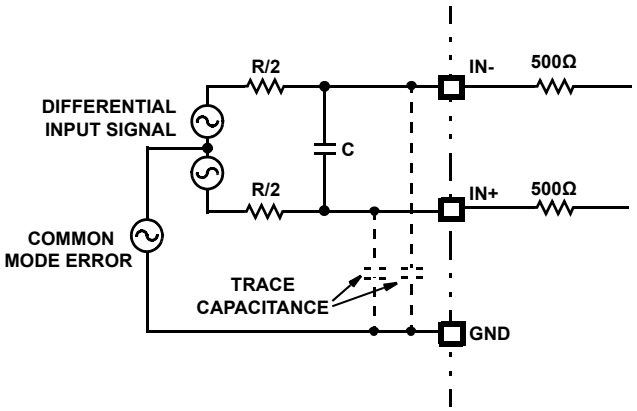


FIGURE 35. INPUT DIFFERENTIAL LOW PASS FILTER AND PARASITIC CAPACITANCE

Input Common Mode Rejection Considerations

The ISL28617 is capable of a very high level (120dB) of CMRR performance from DC to as high as 1kHz. (Figure 1; CMRR vs Frequency). This high level of performance over frequency is made possible by the high common mode input impedance (80GΩ) but requires careful attention to the matching of the IN+ and IN- external impedances to GND.

A mismatch in the series impedance in conjunction with parasitic capacitance at the IN+ and IN- terminals (Figure 35) will cause a common mode amplitude imbalance that will show up as a differential input signal, rapidly degrading CMRR as the common mode frequency increases.

Maximum CMRR performance is achieved with attention to balancing external components and attention to PC layout.

Layout Guidelines

The ISL28617 is a high precision device with wide band AC performance. Maximizing DC precision requires attention to the layout of the gain resistors. Achieving good AC response requires attention to parasitic capacitance at the gain resistor terminals and CMRR performance over frequency is ensured with symmetrical component placement and layout of the input differential signals to the IN+ and IN- terminals.

To ensure the highest DC precision, the location of the gain resistors and PC trace connections to the Kelvin connections are most important. Proper Kelvin connections remove trace resistance errors so that the amplifier gain accuracy and gain temperature coefficients are determined by the gain resistor matching tolerance. Interconnect constraints preclude mounting the gain resistors next to each other, so they should be located on either side of the ISL28617 and as close to the device as

possible. The Kelvin connections are formed at the junction of the sense pins ($\pm R_{IN}$SENSE, $\pm R_{FB}$SENSE) and the gain resistor current drive terminals ($\pm R_{IN}$, $\pm R_{FB}$) terminals. This junction should be made at the terminal pads directly under the ends of each resistor.

Reduced trace lengths that maintain DC accuracy are also important for minimizing the capacitance that can degrade AC stability. This is especially true at gains less than 1. Layout techniques for precision applications using larger size precision gain resistors at very low gains (G = 0.1V/V) include removing a section of the underlying PC ground plane directly under the gain resistor terminals and body.

Layout guidelines for high CMRR include matching trace lengths and symmetrical component placement on the circuit that connects the signal source to the IN+ and IN- pins. This ensures matching of the IN+ and IN- input impedances (Figure 35).

Power Supply Decoupling

Standard power supply decoupling consists of a single 0.1µF 50V ceramic capacitor at the power supply terminals located as close to the device as possible. In applications where the input and output supplies are strapped to the same voltage ($V_{EE} = V_{EO}$, $V_{CC} = V_{CO}$) the connection point should be as close to the device as possible, with a single 0.1µF 50V ceramic capacitor at the junction. Applications using separate supplies require 0.1µF 50V ceramic decoupling capacitors at each power supply terminal.

Estimating Amplifier DC and Noise Performance

The gain resistor ohmic values and ratios are all that is required to estimate DC offset and noise. The following sections illustrate methods to calculate DC offset and noise performance. These estimates are useful for optimizing resistor values for noise and DC offset.

Calculating DC Offset Voltage

Output offset voltage, like output noise, has several contributors. Also similar to output noise, the major offset contributor depends on the gain configuration. In high-gain, $V_{OS(I)}$ dominates, while in low-gain, offset due to I_{ERR} dominates.

The summation of DC offsets to arrive at total DC offset error is performed in two ways. Equation 13 is a simple addition of the DC offsets appearing at the output and is useful when defining the minimum to maximum range of offset that can be expected. The drawback is that the result defines the corner of the corner of the error box and not a typical value given that these sources are uncorrelated.

$$V_{OS}(RTO) = [(A_V \times V_{OS(I)}) + (V_{OS(FB)}) + (I_{ERR} \times R_{FB})] \quad \text{(EQ. 13)}$$

Equation 14 expresses the total DC error as the rms, or square root of the sum of the squares to provide an estimate of a typical value.

$$V_{OS}(RTO)TYP = \sqrt{[(A_V \times V_{OS(I)})^2 + (V_{OS(FB)})^2 + (I_{ERR} \times R_{FB})^2]} \quad \text{(EQ. 14)}$$

Equation 15 converts the output offset error range (Equation 13) to an input referred error range [V_{OS}(RTI)] and enables a comparison with the DC component of the input signal.

$$V_{OS}(RTI) = [(V_{OS(I)}) + (V_{OS(FB)}/A_V) + (I_{ERR} \times R_{FB})/A_V] \quad \text{(EQ. 15)}$$

Similarly, Equation 16 shows the typical DC offset value (Equation 14) referred to the input.

$$V_{OS}(RTI)TYP = \sqrt{[(V_{OS(I)})^2 + (V_{OS(FB)}/A_V)^2 + (I_{ERR} \times R_{FB})/A_V)^2]} \quad \text{(EQ. 16)}$$

NOTE: These results are summarized in Table 1.

Calculating Noise Voltage

The calculation of noise spectral density at the output [e_N(RTO)] from all noise sources is given by Equations 17 and 18:

$$e_N(RTO) = \sqrt{[(A_V \times e_N(I))^2 + (2 \times A_V \times i_N(I) \times 500\Omega)^2 + (A_V)^2 \times (4kT \times R_{IN}) + (4kT \times R_{FB}) + (R_{FB} \times i_N(I_{ERR}))^2 + (e_N(FB))^2]} \quad \text{(EQ. 17)}$$

Then converts the output noise to the input referred value when evaluating the input signal to noise ratio.

$$e_N(RTI) = e_N(RTO)/A_V \quad \text{(EQ. 18)}$$

Table 2 provides examples of the noise contribution of each source by circuit gain and output voltage span. In a high-gain configuration, the input noise is the dominant noise source. In a low-gain configuration, the noise voltage from the product of the internal noise current, $I_{N(err)}$ and the feedback resistor, R_{FB} dominates. The contribution of the internal noise current, $I_{N(err)}$ increases in proportion to R_{FB}, but the corresponding increase in output voltage with R_{FB} keeps the ratio of this noise voltage to output voltage constant.

TABLE 1. COMPUTING TYPICAL OUTPUT OFFSET VOLTAGE RANGES

A_V	$V_{O(LIN)}$	R_{IN} (kΩ)	R_{FB} (kΩ)	A_V x V_{OS}(I) (µV) (Note 11)	V_{OS}(FB) (µV) (Note 11)	I_{ERR} (5nA) x R_{FB} (µV) (Note 11)	V_{OS}(RTO) (µV) (Equation 13)	V_{OS}(RTI) (µV) (Equation 15)	TYPICAL V_{OS}(RTO) (µV) (Equation 14)	TYPICAL V_{OS}(RTI) (µV) (Equation 16)
1	±2.5	30	30	±30	±400	±150	±580		428	
1	±10	120	120	±15	±400	±600	±1015		721	
100	±2.5	0.3	30	±1500	±400	±150	±2000	±20	1560	15.6
100	±10	1.2	120	±1500	±400	±600	±2500	±25	1669	16.7

NOTE:

11. Chosen for illustration purposes and does not reflect actual device performance.

TABLE 2. 1kHz INPUT NOISE AND THERMAL NOISE CONTRIBUTIONS

A_V	R_{IN} (kΩ)	R_{FB} (kΩ)	A_V x e_N(I) (nV/√Hz)	2 x A_V x $i_{N(I)}$ x 500Ω (nV/√Hz)	A_V x √(4kT x R_{IN}) (nV/√Hz)	√(4kT x R_{FB}) (nV/√Hz)	R_{FB} x i_N(I_{ERR}) (nV/√Hz)	e_N(FB) (nV/√Hz)	e_N (RTO) OUTPUT REFERRED NOISE (nV/√Hz)	e_N (RTI) INPUT REFERRED NOISE (nV/√Hz)
1	30	30	8.6	0.15	22.3	22.3	78	8.6	86	
1	120	120	8.6	0.15	44.6	44.6	300	8.6	307	
100	0.3	30	860	15	223	22.3	78	8.6	892	8.9
100	1.2	120	860	15	446	44.6	300	8.6	1015	10.15

NOTE:

12. e_N and i_N values are chosen for illustration purposes and may not reflect actual device performance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
May 27, 2015	FN6562.3	The units of the Y axis on Figures 8, 9, 14, 15 changed from "mV" to “µA” and Figure 16 changed from "mA" to "µA. On page 15, under EXAMPLE 1, added the following after the first sentence: “The sensor signal output is at a much lower voltage level”.
November 17, 2014	FN6562.2	Corrected Typo under “Recommended Operating Conditions” on page 4 from “V_{E+} to V_{EO}”. Removed Important note (*All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*) on page 4 as Note 6 covers this. Updated About Intersil verbiage.
October 17, 2013	FN6562.1	Added a description to the “Related Literature” on page 1. “Thermal Information” on page 4: Added theta jc (top) = 28C/W. Added two new graphs for common mode range vs output voltage (Figure 17 and 18).
May 25, 2012	FN6562.0	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

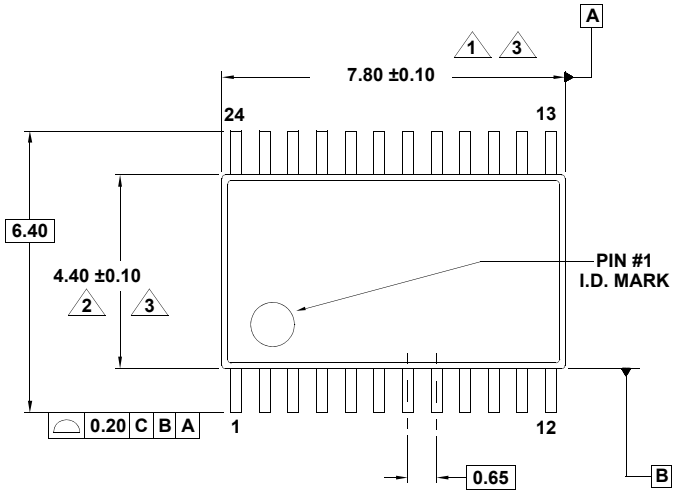
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

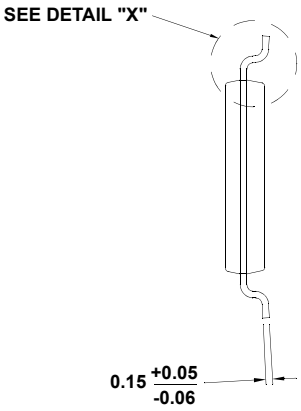
M24.173

24 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

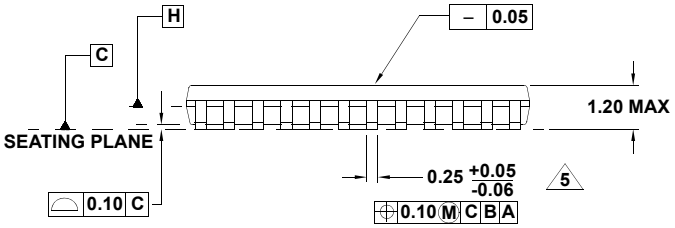
Rev 1, 5/10



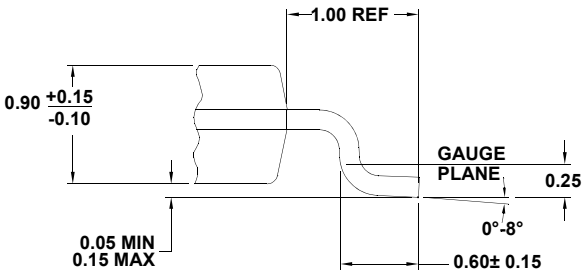
TOP VIEW



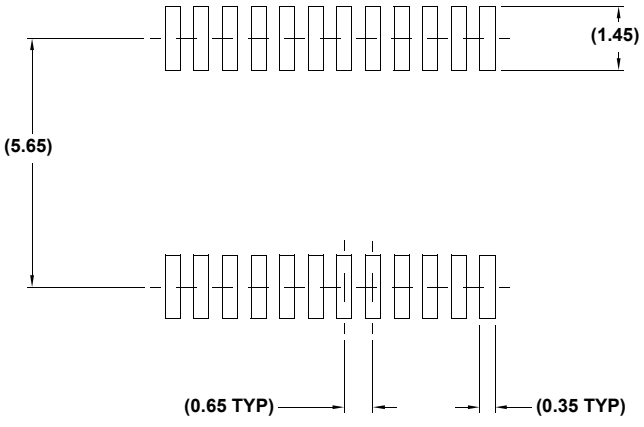
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.