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January 2015

FDMC86340ET80

N-Channel Shielded Gate Power Trench® MOSFET

80 V, 68 A, 6.5 mΩ

Features

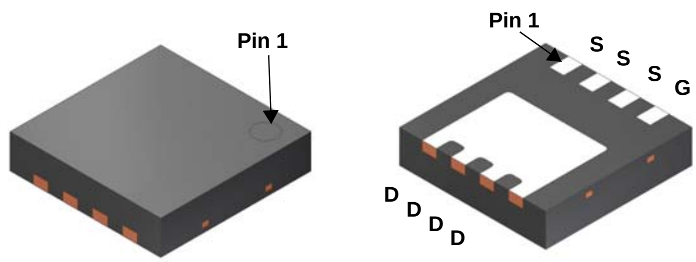
- Extended T_J rating to 175°C
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 6.5 mΩ at V_{GS} = 10 V, I_D = 14 A
- Max $r_{DS(on)}$ = 8.5 mΩ at V_{GS} = 8 V, I_D = 12 A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

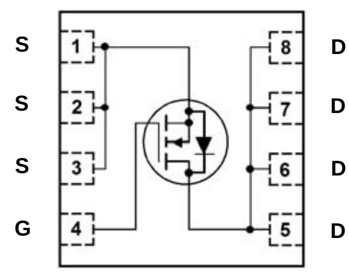
- DC-DC Conversion



Top

Bottom

Power 33



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter				Ratings	Units
V_{DS}	Drain to Source Voltage				80	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	-Continuous	T_C = 25 °C	(Note 5)	68	A
		-Continuous	T_C = 100 °C	(Note 5)	48	
		-Continuous	T_A = 25 °C	(Note 1a)	14	
		-Pulsed		(Note 4)	316	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	216	mJ
P_D	Power Dissipation		T_C = 25 °C		65	W
	Power Dissipation		T_A = 25 °C	(Note 1a)	2.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86340ET	FDMC86340ET80	Power33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		46		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.4	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 14 A		5.0	6.5	mΩ
		V_{GS} = 8 V, I_D = 12 A		6.0	8.5	
		V_{GS} = 10 V, I_D = 14 A, T_J = 125 °C		8.5	11	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 14 A		36		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		2775		pF
C_{oss}	Output Capacitance			468		pF
C_{rss}	Reverse Transfer Capacitance			15		pF
R_g	Gate Resistance		0.1	0.7	2.1	Ω

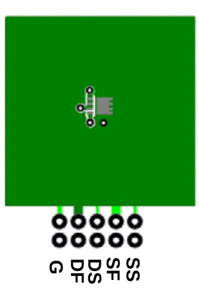
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 14 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		20	32	ns
t_r	Rise Time			7.9	16	ns
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns
t_f	Fall Time			5.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 40 V, I_D = 14 A	30	38	49	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 8 V; V_{DD} = 40 V, I_D = 14 A	20	31	44	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 14 A		14		nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 40 V, I_D = 14 A		8.0		nC
Q_{oss}	Output Charge	V_{DD} = 40 V, V_{GS} = 0 V		42		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 14 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 14 A, di/dt = 100 A/μs		41	66	ns
Q_{rr}	Reverse Recovery Charge			25	40	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 216 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 12 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 37 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted

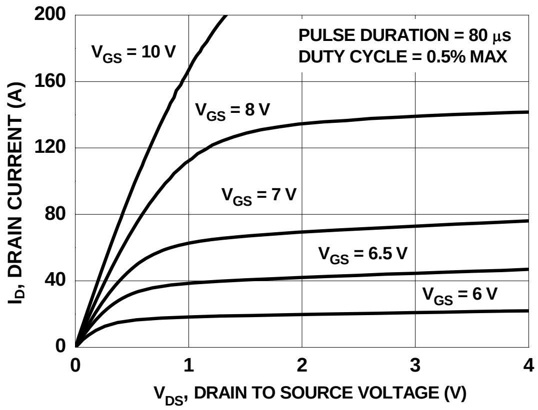


Figure 1. On-Region Characteristics

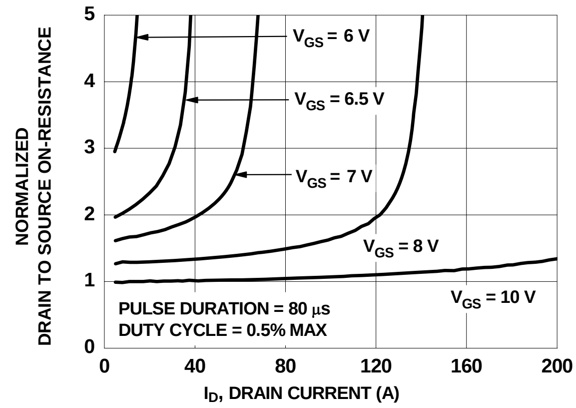


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

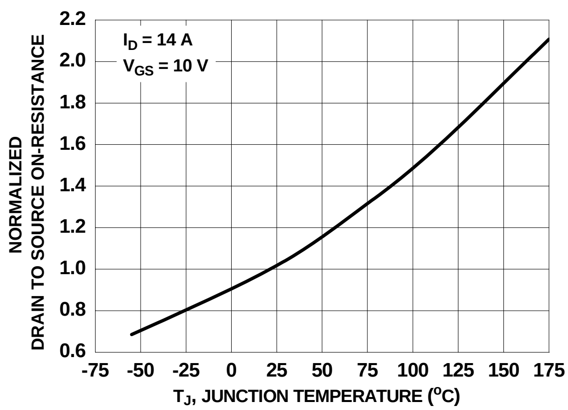


Figure 3. Normalized On-Resistance vs Junction Temperature

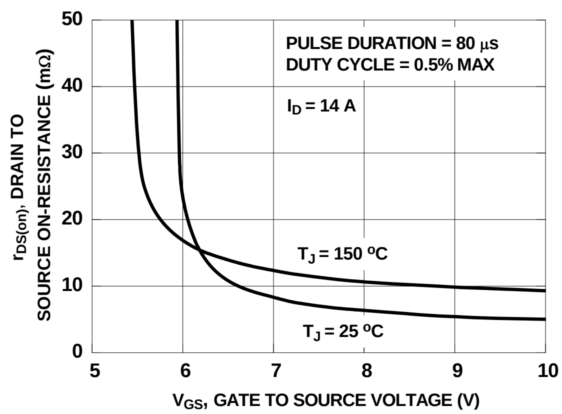


Figure 4. On-Resistance vs Gate to Source Voltage

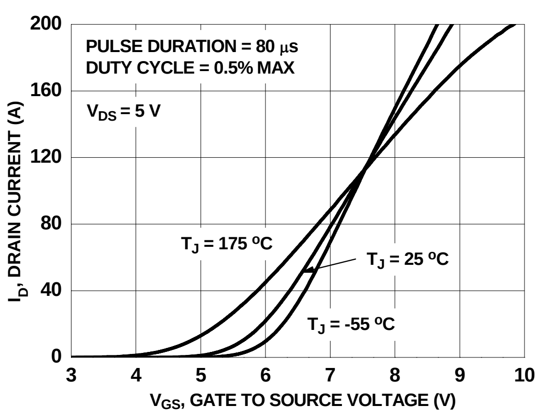


Figure 5. Transfer Characteristics

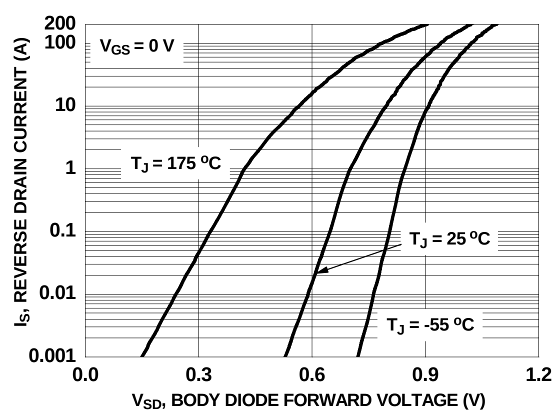


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

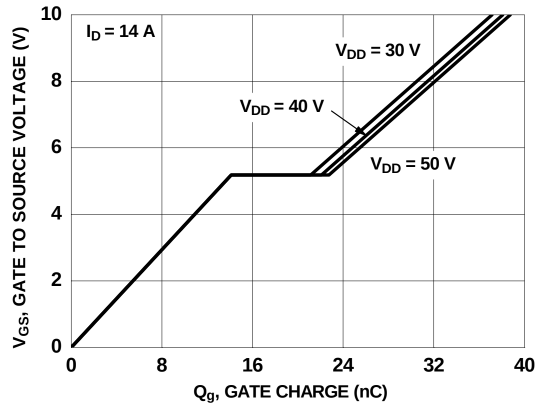


Figure 7. Gate Charge Characteristics

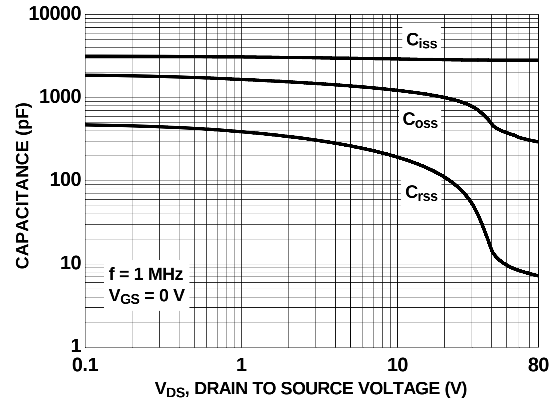


Figure 8. Capacitance vs Drain to Source Voltage

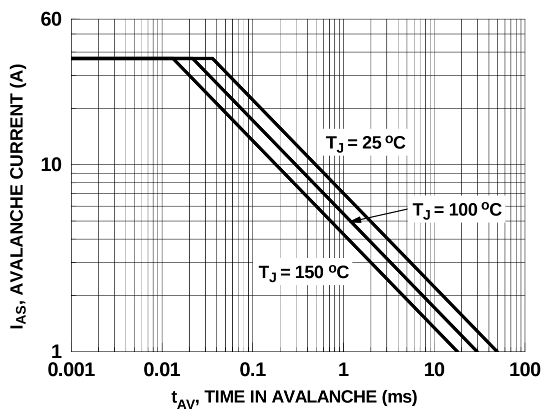


Figure 9. Unclamped Inductive Switching Capability

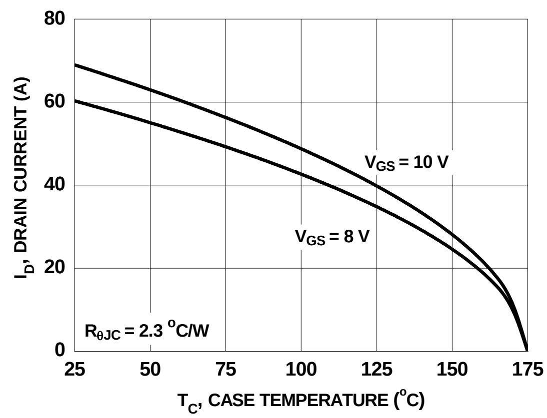


Figure 10. Maximum Continuous Drain Current vs Case Temperature

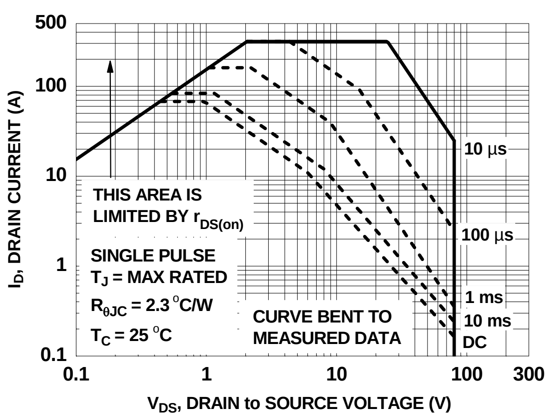


Figure 11. Forward Bias Safe Operating Area

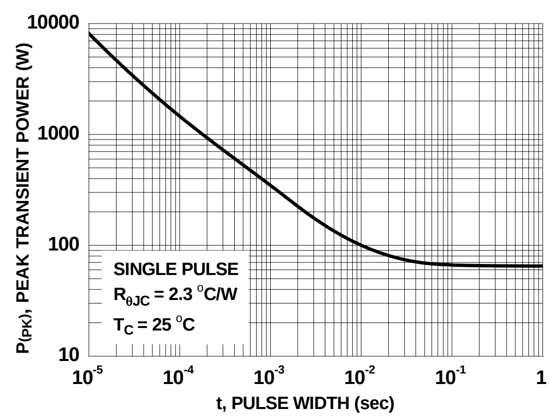


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

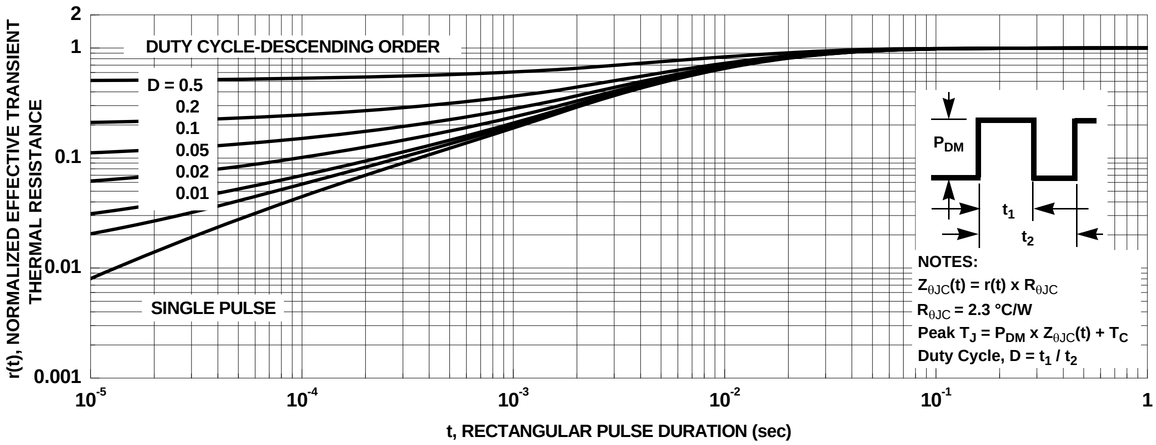
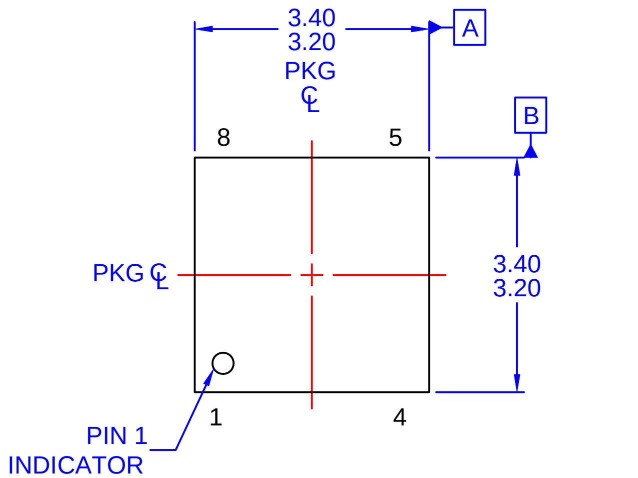
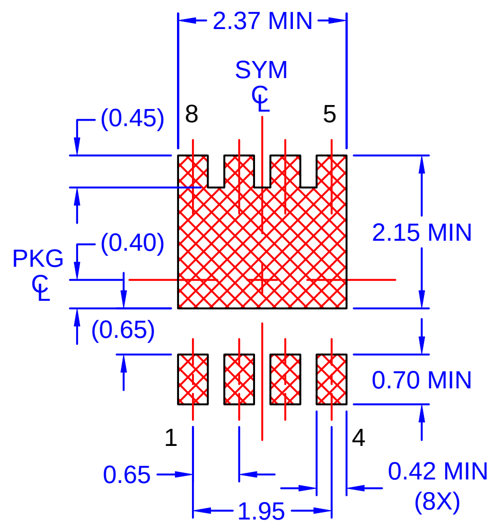


Figure 13. Junction-to-Case Transient Thermal Response Curve





LAND PATTERN
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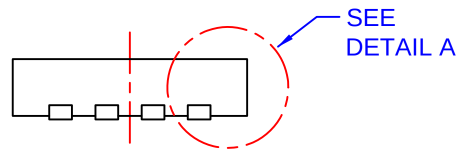

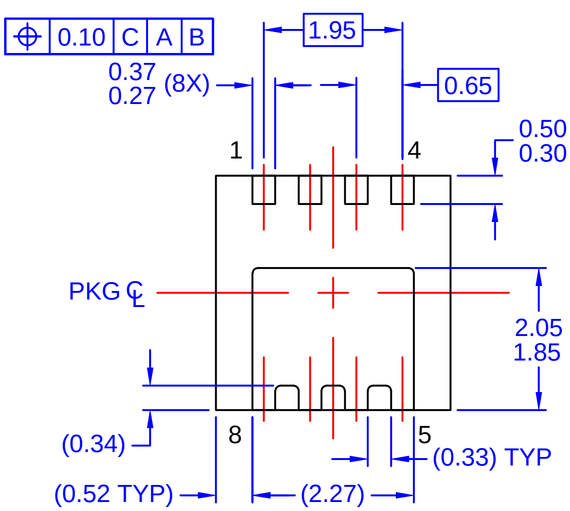

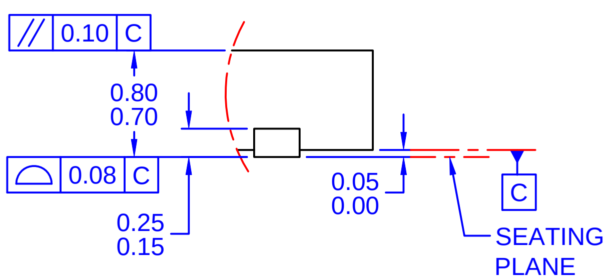

DETAIL A
SCALE: 2X

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