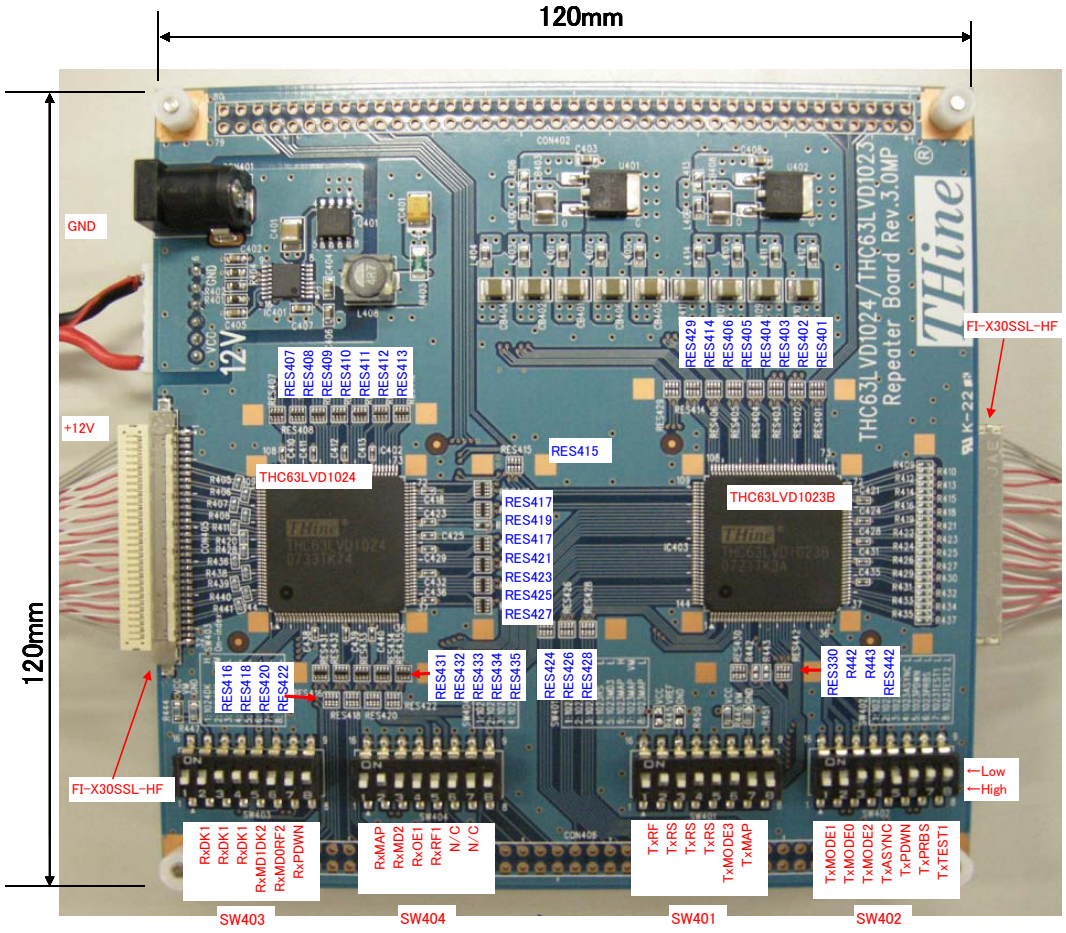
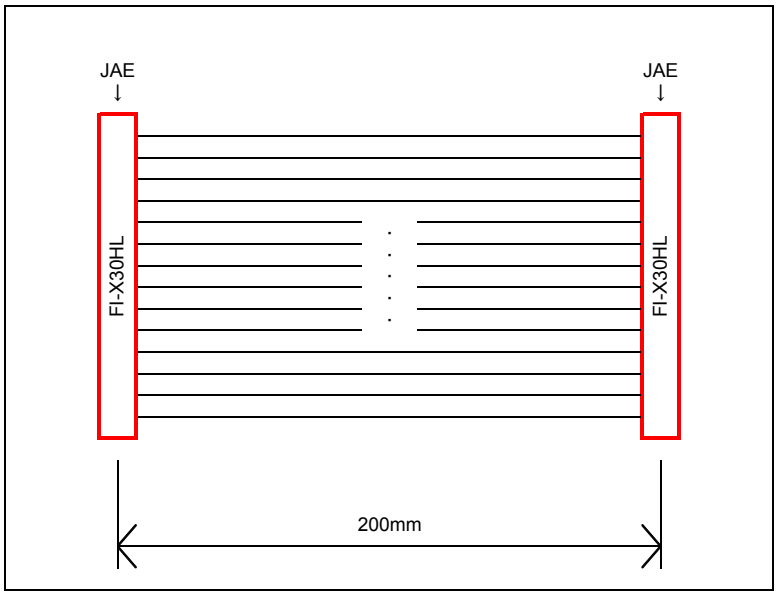
Description

t=1.6mm



LVDS-Cable Type.



SW401 Setting

* Def. : Default Setting

SW Pin#	* Def.	NodeName	THC63LVD1023B IC Pin#	PinName	Description
1	H	TxRF	21	R/F	Input Clock Triggering Edge Select. H : Rising edge, L : Falling edge
2	L	TxRS	22	RS	LVDS swing mode, VREF select.
3	H				
4	H				
5	L	TxMODE3	23	MODE3	Input port switching function enable when MODE<1:0>=HL(Single-in/Dual-out Mode). H or Open: Port switch disable. L: Port switch enable.
6	L	TxMAP	24	MAP	LVDS mapping table select.
7	H				
8	H				

SW-Pin# 2	SW-Pin# 3	SW-Pin# 4	RS	LVDS Swing	Small Swing Input Support
L	H(open)	H(open)	VIHM	350mV	N/A
H(open)	L	H(open)	VIMM	350mV	RS=VREFa
H(open)	H(open)	L	VILM	200mV	N/A

a) VREF is Input Reference Voltage.

SW-Pin# 6	SW-Pin# 7	SW-Pin# 8	RS	Mapping Mode
L	H(open)	H(open)	VIHM	Mapping MODE1
H(open)	L	H(open)	VIMM	Mapping MODE2
H(open)	H(open)	L	VILM	Mapping MODE3

SW402 Setting

* Def. : Default Setting

SW Pin#	* Def.	NodeName	THC63LVD1023B IC Pin#	PinName	Description
1	H	TxMODE1	25	MODE1	Pixel Data Mode.
2	H	TxMODE0	26	MODE0	
3	L	TxMODE2	27	MODE2	The use of these multi-function depends on the setting of MODE<1:0> or ASYNC. ASYNC=H(MODE<1:0>=Don't care.) H: Cross point switching enable. L: Cross point switching disable. ASYNC=L MODE<1:0>=HH(Single-in/Single-out Mode) H: Distribution function enable. L: Distribution function disable. MODE<1:0>=HL(Single-in/Dual-out Mode) H: DDR (Double Edge input) function enable. L: DDR (Double Edge input) function disable.
4	L	TxASYNC	28	ASYNC	Asynchronous function enable. H : Asynchronous mode enable.(MODE<1:0>=Disable) L : Asynchronous mode disable.(MODE<1:0>=Enable)
5	H	TxPDWN	30	/PDWN	H: Normal operation, L: Power down (all outputs are Hi-Z)
6	L	TxPRBS	31	PRBS	PRBS(Pseudo-Random Binary Sequence) generator is active in order to evaluate eye patterns when MODE<1:0> = LL(Dual-in/Dual-out mode) or ASYNC=H H: PRBS generator is enable. L: Normal Operation
7	L	TxTEST1	32	Reserved	Must be tied to GND.
8	H	TxTEST2	33	N/C	Must be Open.

MODE1	MODE0	Mode
H	H	Single Link(Single-in/Single-out)
H	L	Single Link(Single-in/Dual-out)
L	H	Dual Link(Dual-in/Single-out)
L	L	Dual Link(Dual-in/Single-out)

SW403 Setting

* Def. : Default Setting

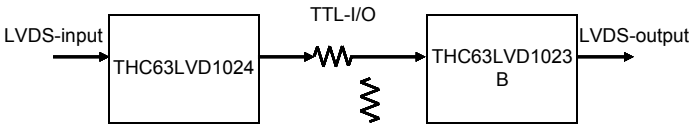
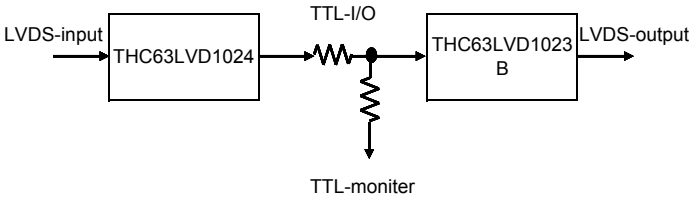
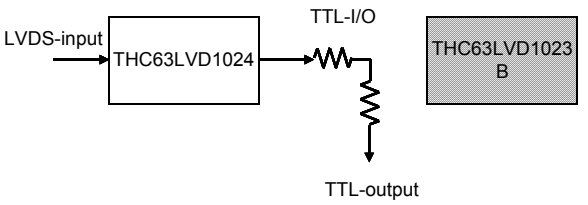
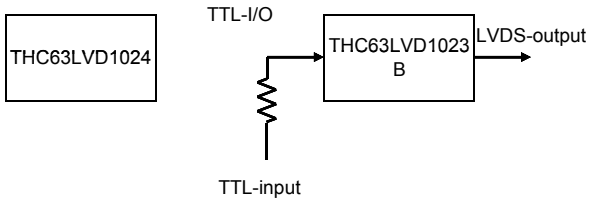
<table>
<tr><th rowspan="2">SW Pin#</th><th rowspan="2">* Def.</th><th rowspan="2">NodeName</th><th colspan="3">THC63LVD1024</th></tr>
<tr><th>IC Pin#</th><th>PinName</th><th>Description</th></tr>
<tr><td>1
2
3</td><td>H
H
L</td><td>RxDK1</td><td>7</td><td>DK</td><td>Output Clock Delay Timing Select.
tDOUT=Output Data Cycle
<table>
<tr><th rowspan="2">MODE[1:0]</th><th colspan="3">SW-Pin#</th><th rowspan="2">Offset[nsec]</th></tr>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td rowspan="3">LL
HH
HL</td><td>L</td><td>H(open)</td><td>H(open)</td><td>$6\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>L</td><td>H(open)</td><td>$-6\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>H(open)</td><td>L</td><td>0</td></tr>
<tr><td rowspan="3">LH</td><td>L</td><td>H(open)</td><td>H(open)</td><td>$7\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>L</td><td>H(open)</td><td>$-7\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>H(open)</td><td>L</td><td>0</td></tr>
</table></td></tr>
<tr><td>4
5</td><td>L
L</td><td>RxMD1DK2
RxMD0RF2</td><td>6
5</td><td>MODE1
MODE0</td><td>Pixel Data Mode.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>H</td><td>H</td><td>Single Link(Single-in/Single-out)</td></tr>
<tr><td>H</td><td>L</td><td>Single Link(Single-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Dual Link(Dual-in/Single-out)</td></tr>
<tr><td>L</td><td>L</td><td>Dual Link(Dual-in/Single-out)</td></tr>
</table></td></tr>
<tr><td>6</td><td>H</td><td>RxPDWN</td><td>4</td><td>/PDWN</td><td>Power down and Output Control.
H : Normal operation
L : Power down</td></tr>
<tr><td>7</td><td>H</td><td>RxOE2</td><td>3</td><td>Reserved</td><td>Must be tied to VCC.</td></tr>
<tr><td>8</td><td>L</td><td>RxTEST</td><td>144</td><td>LGND</td><td>Ground Pins for LVDS inputs.</td></tr>
</table>

SW404 Setting

* Def. : Default Setting

<table>
<tr><th rowspan="2">SW Pin#</th><th rowspan="2">* Def.</th><th rowspan="2">NodeName</th><th colspan="3">THC63LVD1024</th></tr>
<tr><th>IC Pin#</th><th>PinName</th><th>Description</th></tr>
<tr><td>1</td><td>H</td><td>RxMAP</td><td>11</td><td>MAP</td><td>LVDS mapping table select.
H : Mapping Mode1
L : Mapping Mode2</td></tr>
<tr><td>2</td><td>L</td><td>RxMD2</td><td>10</td><td>MODE2</td><td>DDR function enable.
<table>
<tr><th>MODE<1:0></th><th>MODE2</th><th>Mode</th></tr>
<tr><td rowspan="2">LH</td><td>H</td><td>DDR (Double Edge Output) function enable.</td></tr>
<tr><td>L</td><td>DDR (Double Edge Output) function disable.</td></tr>
<tr><td>LL
HL
HH</td><td>L</td><td>Must be tied to GND</td></tr>
</table></td></tr>
<tr><td>3</td><td>H</td><td>RxOE1</td><td>9</td><td>OE</td><td>Output Enable.
H : Output enable,
L : Output disable</td></tr>
<tr><td>4</td><td>H</td><td>RxRF1</td><td>8</td><td>R/F</td><td>Output Clock Triggering Edge Select.
H : Rising edge.
L : Falling edge.</td></tr>
<tr><td>5</td><td>H</td><td>N/C</td><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">Non Connected</td></tr>
<tr><td>6</td><td>H</td><td>N/C</td></tr>
<tr><td>7</td><td>H</td><td>N/C</td></tr>
<tr><td>8</td><td>H</td><td>N/C</td></tr>
</table>

Measures Type

#	Type	Un-Mount	0Ω-Mount	33Ω-Mount
1		RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 **RES418 R443**		RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 **RES421**
2			RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 RES418 R443	RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 RES421
3		THC63LVD1023B	RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 RES418 R443	RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 RES421
4		RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 RES421	RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 RES418 R443	

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7. Please note that this product is not designed to be radiation-proof.
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