PCF1179C

4-digit duplex LCD car clock

Rev. 3 — 12 February 2015 Product data sheet

1. General description

The PCF1179C is a single chip, 4.19 MHz car clock circuit providing hours, minutes, and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD).

Two external single-pole, single-throw push buttons accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

2. Features and benefits

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for a good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: −40 °C to +85 °C
- 28-lead plastic SMD (SO28)
- 4 Hz set mode.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF1179CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF1179CT	PCF1179CT,112	935059760112	Tube	1
PCF1179CT	PCF1179CT,118	935059760118	Reel Pack, SMD, 13 inch	1

4. Marking

Table 3. Marking codes

Type number	Marking code
PCF1179CT	PCF1179CT

5. Block diagram

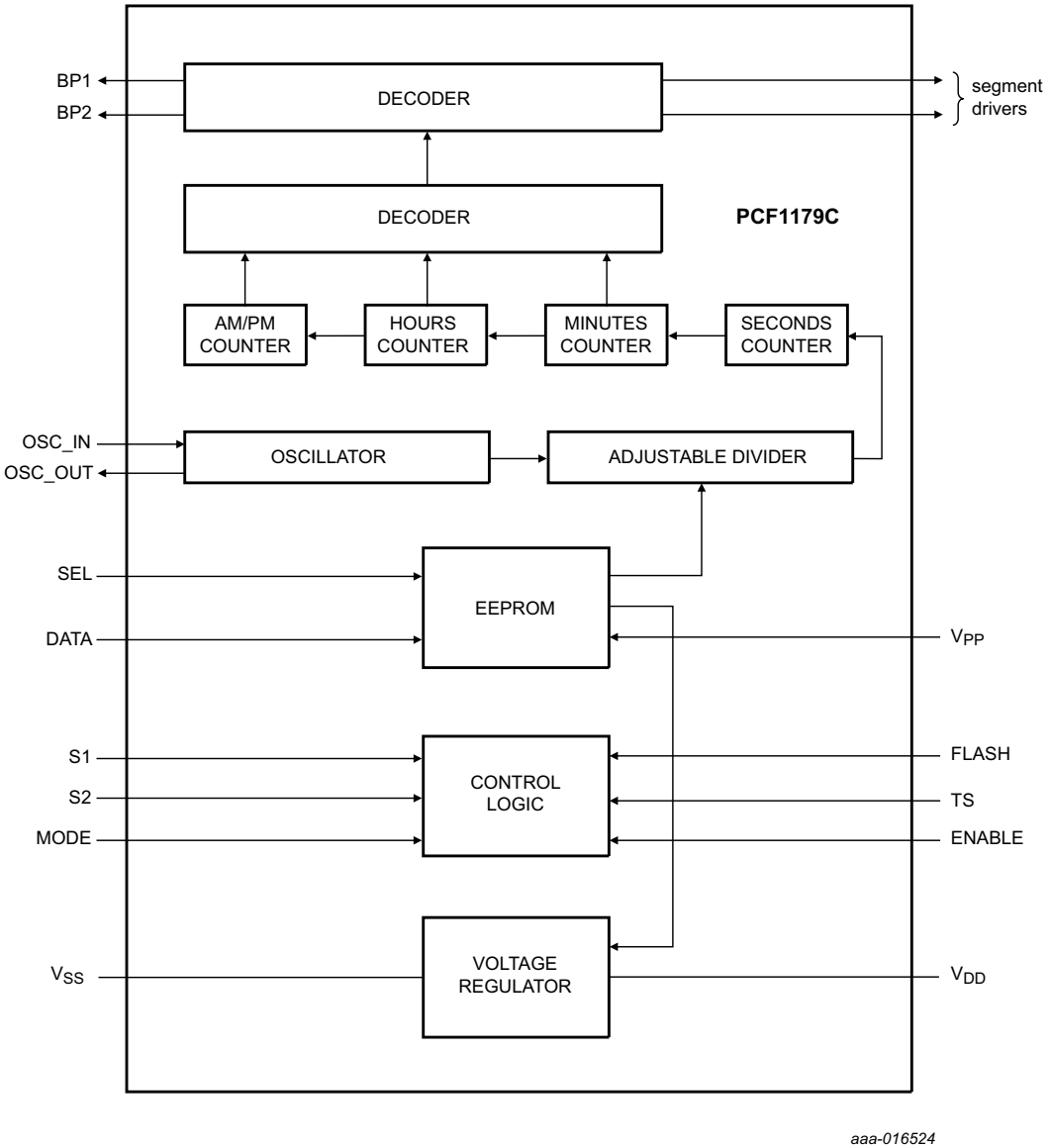
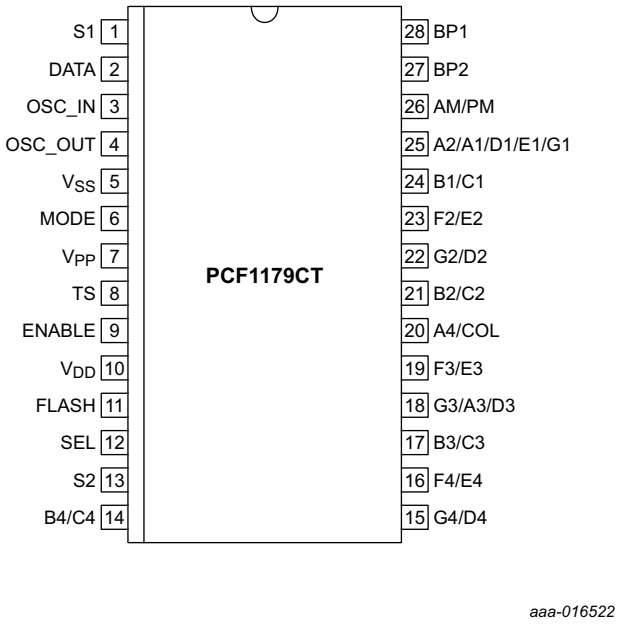


Fig 1. Block diagram of PCF1179C

6. Pinning information

6.1 Pinning



Top view. For mechanical details, see Figure 9.

Fig 2. Pin configuration of PCF1179CT

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
S1	1	hour adjustment input
DATA	2	EEPROM data input
OSC_IN	3	oscillator input
OSC_OUT	4	oscillator output
V_{SS}	5	negative supply voltage
MODE	6	12/24-hour mode select input
V_{PP}	7	programming voltage input
TS	8	test speed-up mode input
ENABLE	9	enable input (for S1 and S2)
V_{DD}	10	positive supply voltage
FLASH	11	colon option input
SEL	12	EEPROM select input
S2	13	minute adjustment input
B4/C4	14	segment drivers
G4/D4	15	
F4/E4	16	
B3/C3	17	
G3/A3/D3	18	
F3/E3	19	
A4/COL	20	
B2/C2	21	
G2/D2	22	
F2/E2	23	
B1/C1	24	
A2/A1/D1/E1/G1	25	
AM/PM	26	
BP2	27	backplane 2
BP1	28	backplane 1

7. Functional description

7.1 Outputs

Typical displays for the PCF1179C are shown in Figure 3.

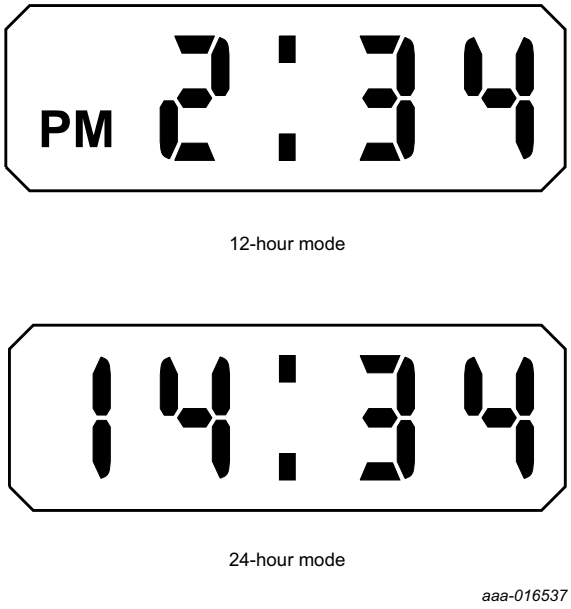


Fig 3. Typical displays for the PCF1179C

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. The segment assignment of the LCD is show in Figure 4.

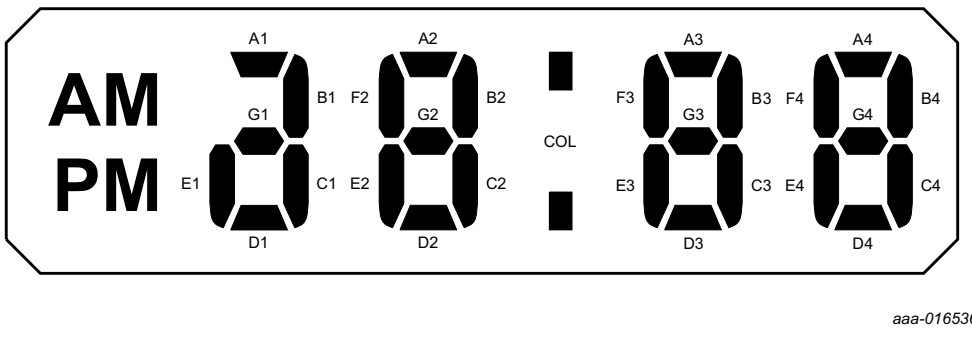


Fig 4. Segment assignment of the LCD

7.2 LCD voltage

Generation of BP1 and BP2 (three-level backplane signals at V_{DD}, $V_{DD}/2$, and 0) and the output signals are shown in Figure 5.

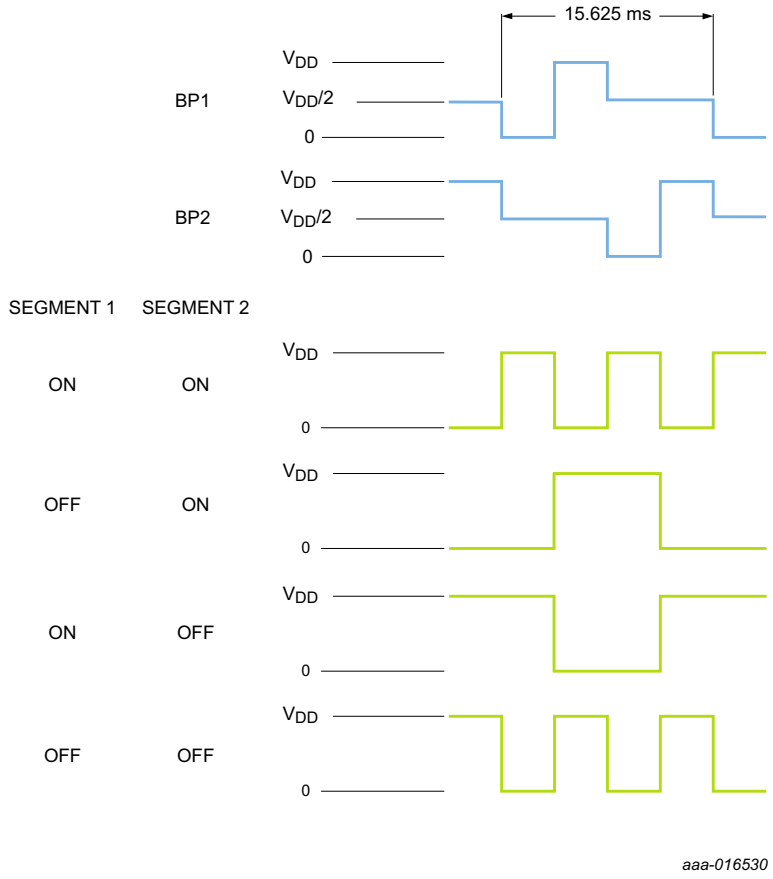


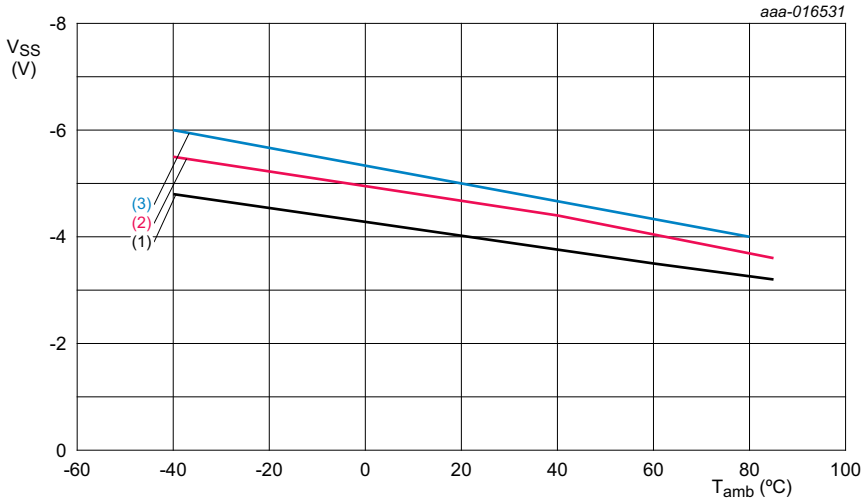
Fig 5. Backplane and segment output signals

The average voltages across the segments are:

1. $V_{ON(RMS)} = 0.79V_{DD}$
2. $V_{OFF(RMS)} = 0.35V_{DD}$

For a good contrast, the adjustable voltage regulator controls the supply voltage (see Figure 6 and Section 7.13) in relation to temperature. For example, when V_{DD} = 4.5 V at +25 °C, then:

- V_{DD} = 3 V to 4 V at +85 °C
- V_{DD} = 5 V to 6 V at −40 °C



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).

(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).

(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig 6. Regulated voltage as a function of temperature (typical)

7.3 12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode changes from 12-hour to 24-hour mode or vice versa.

7.4 Power-on

After connecting the supply, the start-up mode is:

- MODE connected to V_{DD}: 12-hour mode, 1:00 AM.
- MODE connected to V_{SS}: 24-hour mode, 0:00.
- MODE left open-circuit: 24-hour mode, 0:00 or 1:00.

7.5 Colon

If FLASH is connected to V_{DD}, the colon pulses at 1 Hz.

If FLASH is connected to V_{SS}, the colon is static.

7.6 Time setting

The push button inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

7.7 Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting it to V_{SS}.

7.8 Set hours

When S1 is connected to V_{SS}, the hours displayed advances by one and after one second it continues with four advances per second until S1 is released (auto-increment).

7.9 Set minutes

When S2 is connected to V_{SS}, the time displayed in minutes advances by one and after one second it continues with four advances per second until S2 is released (auto-increment). In addition to the minute correction, the seconds counter is reset to zero. Overflow in the minute counter does not have an influence on the hour counter.

7.10 Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing push buttons S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

7.11 Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS}, all counters (seconds, minutes, and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

7.12 EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

7.13 LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP}, see Figure 7. The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage returns to the lowest value.

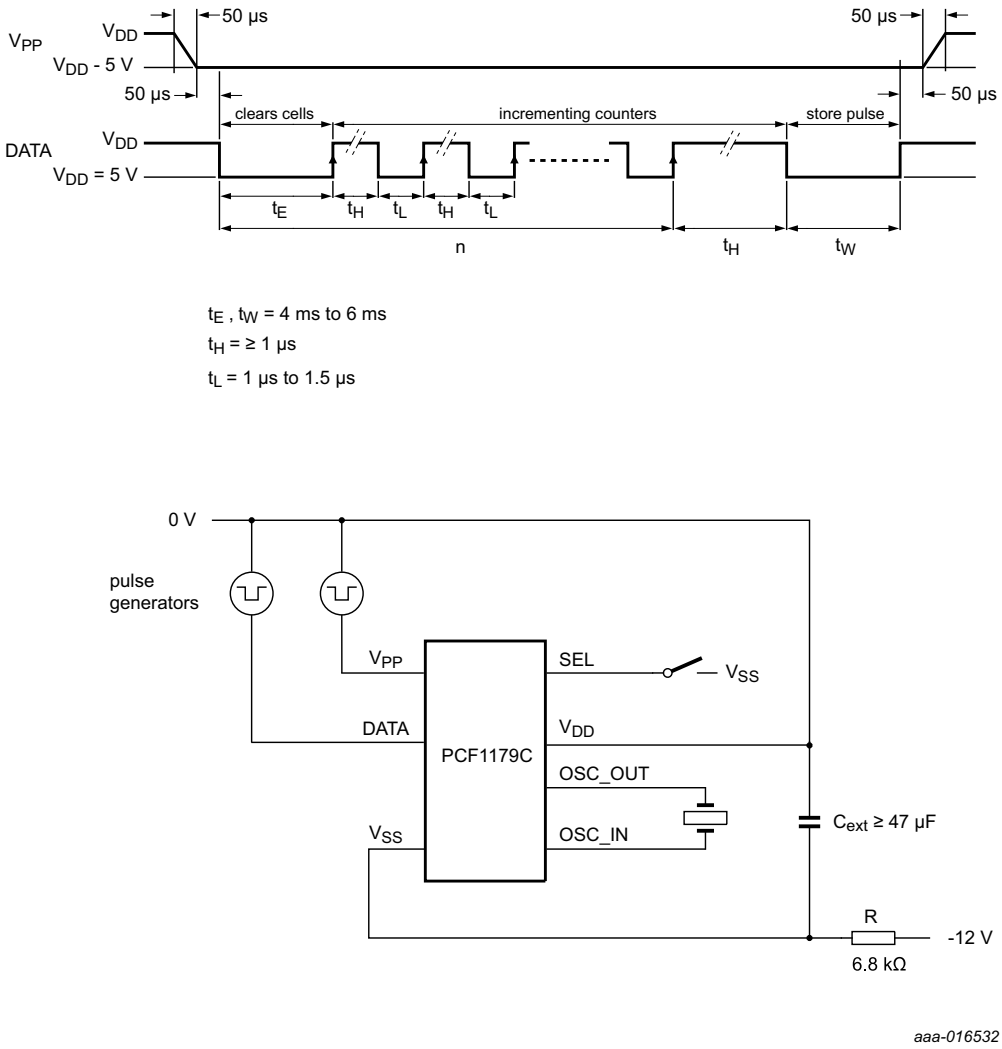


Fig 7. Programming diagram

7.14 Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$) by capacitors at the oscillator input and output, a number (n) of 262 144 Hz pulses are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps, see Figure 7:

1. Set SEL to V_{SS} and a level of $V_{DD} - 5$ V to V_{PP}
2. The quartz-frequency deviation $\Delta f/f$ is measured and (n) is calculated (see Table 5)
3. A first pulse, t_E, is applied to the DATA input. It clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied, the period returns to the lowest value.

5. The backplane period is controlled and then correctly fixed by applying the store pulse t_W
6. Release SEL and V_{PP}.

Table 5. Time calibration

Δt = 7.63 μs; SEL at V_{SS}.

Oscillator-frequency deviation $\Delta f/f$ ($\times 10^{-6}$)	Number of pulses (n)	Backplane period (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
:	:	:
+117.8	31	15.861

8. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	with respect to V_{SS}	-	8	V
I_{DD}	supply current	V_{SS} = 0 V [1]	-	3	mA
V_I	input voltage	all pins except V_{PP}, DATA	−0.3	V_{DD} + 0.3	V
		pins V_{PP}, DATA	−3	V_{DD} + 0.3	V
V_{ESD}	electrostatic discharge voltage	HBM [2]	-	±2000	V
I_{lu}	latch-up current	[3]	-	100	mA
T_{stg}	storage temperature	[4]	−55	+125	°C
T_{amb}	ambient temperature	operating device	−40	+85	°C

[1] Connecting the supply voltage with reverse polarity, does not harm the circuit, provided the current is limited to 10 mA by an external resistor.

[2] Pass level; Human Body Model (HBM), according to Ref. 6 “JESD22-A114”.

[3] Pass level; latch-up testing according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 10 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

10. Characteristics

Table 7. Characteristics

V_{DD} = 3 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ±30 × 10^{-6}; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	-	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	-	-	50	mV
TC	supply voltage variation due to temperature		-	−0.35	-	%/K
		V_{DD} = 4.5 V	-	−16	-	mV/K
I_{DD}	supply current	[1]	700	950	-	µA
C_{EXT}	capacitance	external capacitor	47	-	-	µF
Oscillator						
t_{osc}	start time		-	-	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 × 10^{-6}	110 × 10^{-6}	-
Δf/f	frequency stability	ΔV_{DD} = 100 mV	-	-	1 × 10^{-6}	-
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		-	16	-	pF
C_o	output capacitance		-	27	-	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL, DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	-	-	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	-	700	µA
		during programming	-	500	-	µA
Backplane (HIGH and LOW levels)						
R_{BP}	output resistance	±100 µA	-	-	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	-	-	5	kΩ
LCD						
$V_{offset(DC)}$	DC offset voltage	200 kΩ/1 nF	-	-	50	mV

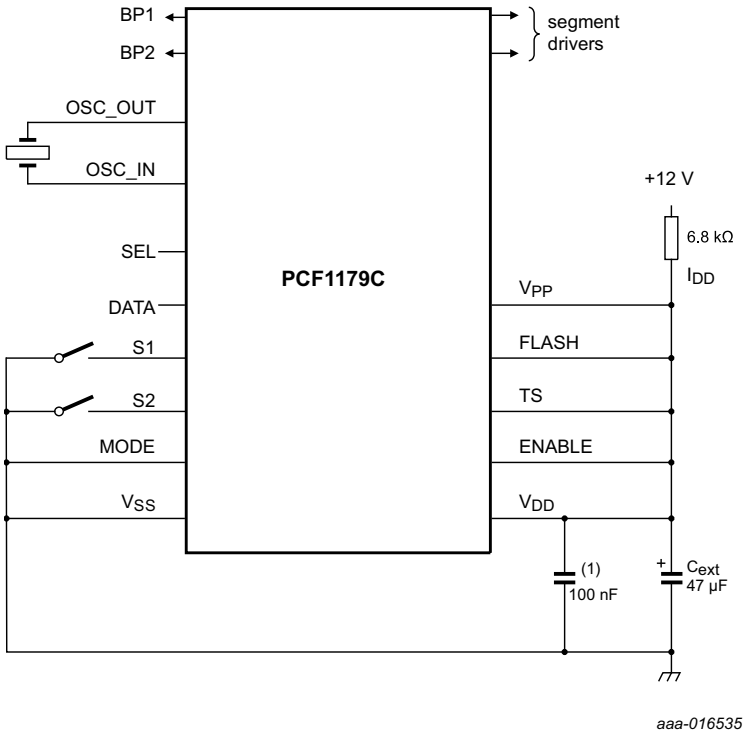
[1] A suitable resistor (R) must be selected (example):

a) V_{DD} = 5 V; R_{max} = (12 V − 5 V)/700 µA = 10 kΩ.

b) V_{DD} = 5 V; R_{typ} = (12 V − 5 V)/1000 µA = 7 kΩ (1000 µA, to have more reserve).

c) I_{DD} must not exceed 3 mA.

11. Application information

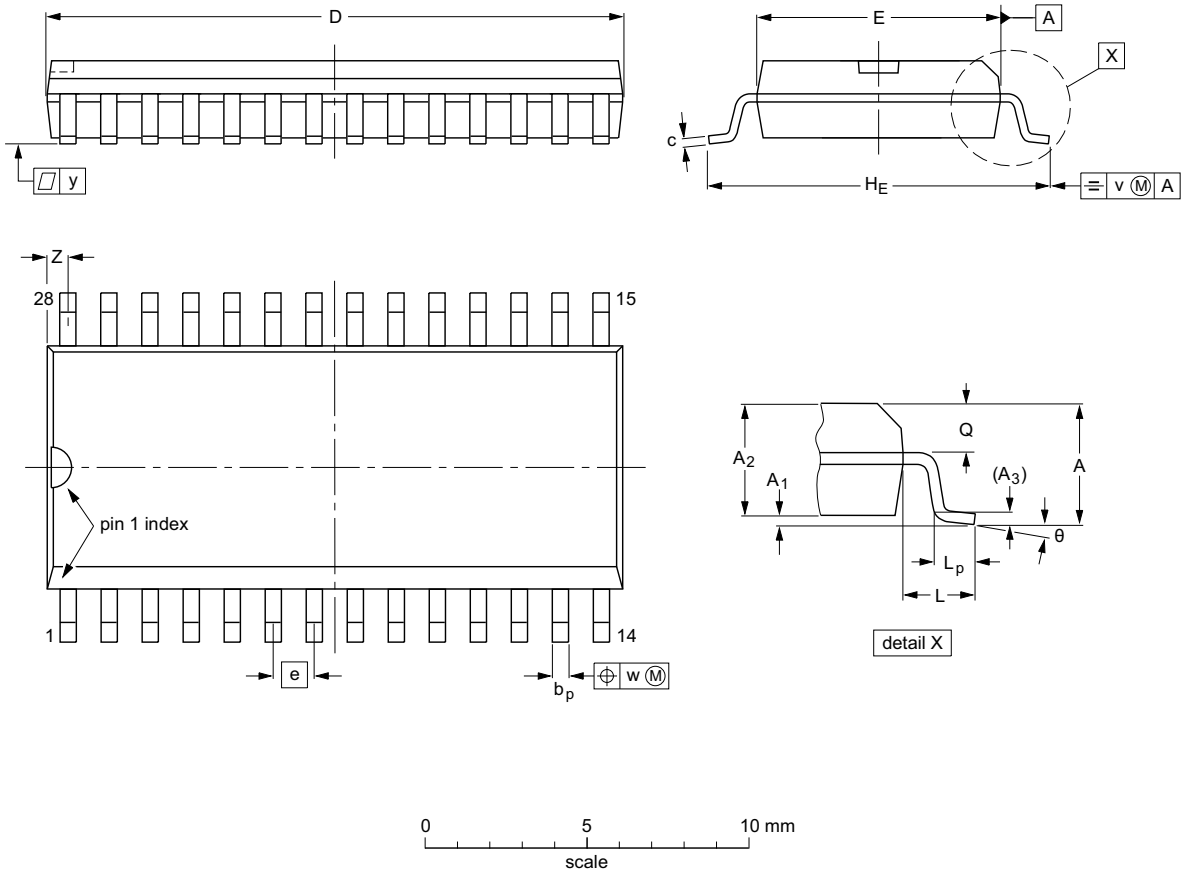


(1) To be mounted close to the IC.

Fig 8. Application diagram

12. Package outline

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT136-1	075E06	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT136-1 (SO28) of PCF1179CT

13. Packing information

13.1 Tape and reel information

For tape and reel packing information, see Ref. 9 “SOT136-1_118” on page 19.

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020D)

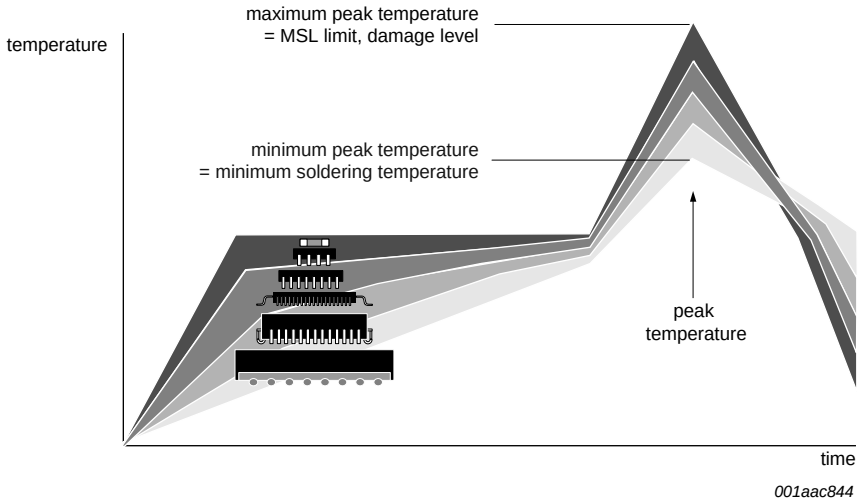
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



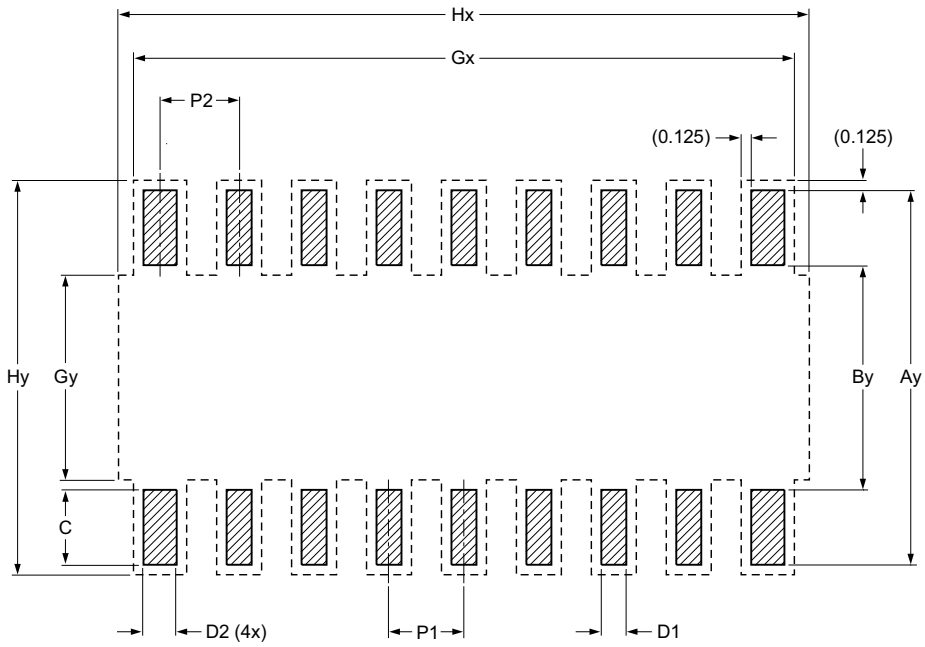
MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

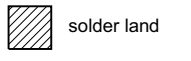
15. Soldering: Footprint information

Footprint information for reflow soldering of SO28 package **SOT136-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	11.200	6.400	2.400	0.700	0.800	17.660	8.600	19.500	11.450

sot136-1_fr

Fig 11. Footprint information for reflow soldering of SOT136-1 (SO28) of PCF1179CT

16. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10853 —** ESD and EMC sensitivity of IC

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **SOT136-1_118 —** SO28; Reel dry pack; SMD, 13", packing information

[10] **UM10569 —** Store and transport requirements

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF1179C v.3	20150212	Product data sheet	-	PCF1179C v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Removed obsolete product types • Fixed typos			

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Bare die — All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP Semiconductors N.V.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Tables

21. Figures

22. Contents

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