Preliminary **AK8998/W/D**

The AK8998 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation. It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8998. The AK8998 is available in a 16-pin QFN package, in wafer form and in a tray.

Features

- **Pressure sensor compensation and excitation IC (Analog output)**
- **Supply voltage current: 7.1mA max @10kHz sampling**
- **Supply voltage: 3.0V±5%, 3.3V±5%, 5.0V±5%**
- **Operating temperature range: -20 to 85ºC**
- **Integrated sensor output compensation (AK8998 Input conversion)**
  - **Offset voltage adjustment**
    - **Adjustment range: Rough ±13 to ±373mV / Fine ±1 to ±34mV @5.0V**
    - **Adjustment step: Rough 2 to 53mV /step / Fine 0.01 to 0.27mV /step @5.0V**
  - **Offset voltage temperature drift adjustment (1st order coefficient)**
    - **Adjustment range: ±0.04 to ±1.23mV/ºC @5.0V**
    - **Adjustment step: 0.2 to 4.8µV/ºC @5.0V**
  - **Output span voltage adjustment (G1, G2, G3)**
    - **Total adjustment range: 5.7 to 261.6mV @5.0V**
    - **G1 adjustment step: 0.95 to 74.7mV /step @5.0V**
    - **G2 adjustment step: 5.7 to 130.8mV /step @5.0V**
    - **G3 adjustment step: 0.01 to 0.40mV /step @5.0V**
  - **Sensitivity temperature drift adjustment (1st order coefficient)**
    - **Adjustment range: -4000ppm/ºC to +2500ppm/ºC or -2500ppm/ºC to +1000ppm/ºC**
    - **Adjustment step: 18ppm/ºC step**
- **Integrated output reference voltage adjustment function**
  - **Adjustment range: 0.02*VDD to 0.98*VDD**
  - **Adjustment step: 10mV /step @5.0V**
- **Integrated sampling frequency switching function: 1kHz, 10kHz**
- **Integrated analog circuit reference voltage stabilizer (Add an external capacitor to AGND pin as needed)**
- **SCF and SMF included for band limitation: fc:1.0kHz, 500Hz, 250Hz**
- **2 wire serial interface (CSCLK, VOUT)**
- **Ratiometric voltage output**
- **Integrated constant voltage source for pressure sensor: 2.2V @ 3.0, 3.3V±5%**
  4.0V or 2.2V @ 5.0V±5%
- **Integrated pressure detectors (x2)**
  - **Detection threshold adjustment control**
    - **Adjustment range: 0.125*VDD to 0.9*VDD**
    - **Adjustment step: 0.025*VDD /step**
  - **Detection threshold external setting function (DET2 / PTH pin use)**
  - **hysteresis voltage adjustment control**
    - **Adjustment range: 0.03*VDD to 0.06*VDD**
    - **Adjustment step: 0.01*VDD /step**
- **Integrated reference voltage & reference current generator**
  - **VREF voltage adjustment control**
    - **Resolution: 3bits**
    - **Adjustment step: 1% /step**

- IREF current adjustment control
  - Resolution: 4bits
  - Adjustment step: 2.8% /step typ.

• Temperature sensor (internal or external)
- Temperature range: -20 to 85 °C
- Internal temperature sensor output voltage adjustment control
  - Resolution: 6 bits
  - Adjustment step: 0.2% /step
- External temperature sensor output voltage adjustment control
  - Resolution: 9 bits（Rough/ Fine=3/6bits）
  - Adjustment step: Rough 10% /step / Fine 0.2% /step
- Integrated external temperature sensor constant current circuit: 50μA typ.

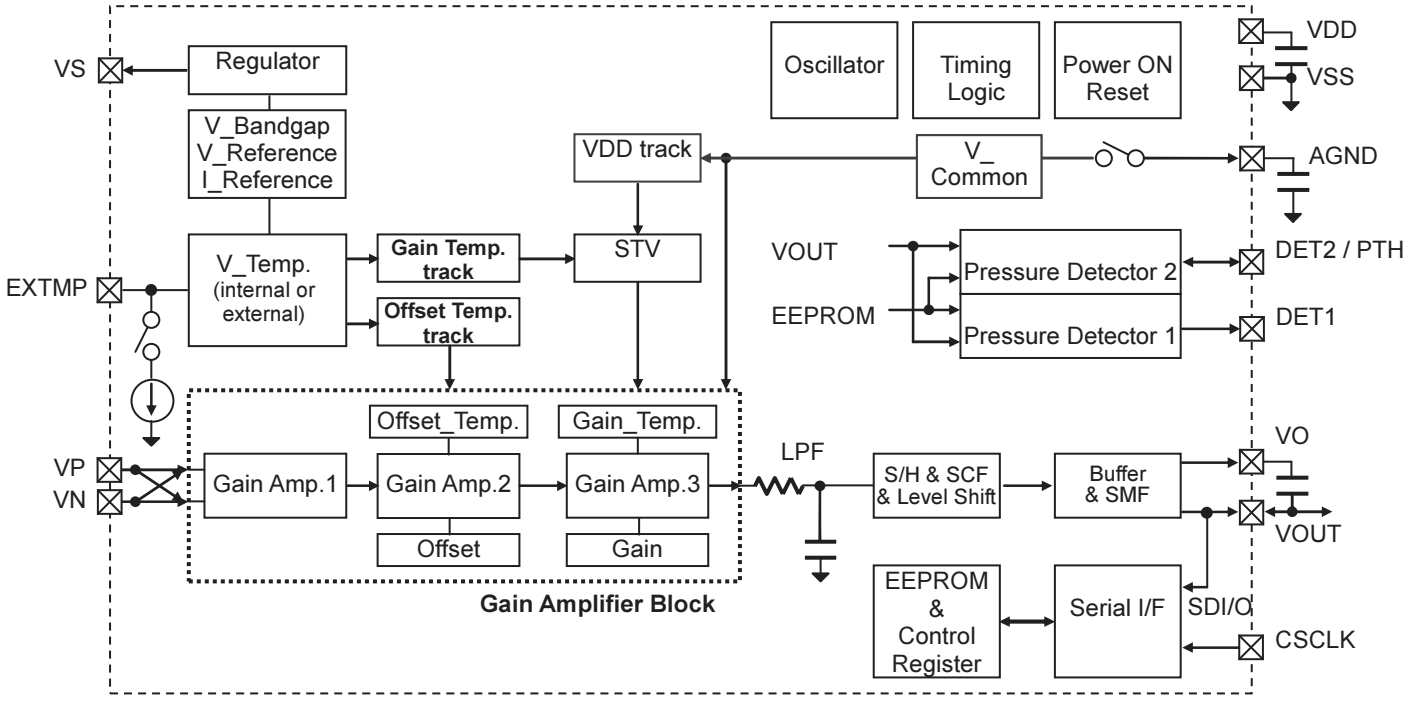
• Integrated oscillator for intermittent operation (1000kHz typ.)
- Oscillating frequency adjustment control
  - Resolution: 4 bits
  - Adjustment step: 5% /step typ.

• Integrated EEPROM for compensation values and control data storage
- Size: 131 bits
- Endurance: 1,000 times or more
- Retention time: 10 years or more @Ta: 85°C

• Supply Type: Tray (Die), Wafer, PKG (UQFN16)

Product name	Supply Type	Comments
AK8998	PKG (UQFN16)	
AK8998W	Wafer	
AK8998D	Tray (Die)	

Block Diagram



Overview

The AK8998 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation.

It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8998.

The internal compensation circuit is accomplished through a 12-bit resolution DAC (Rough: 4bits, Fine: 8bits) to adjust offset voltage, and the primary characteristics compensator for the associated temperature drift, coupled with 13-bit resolution (G1&G2 Gain adjustment: 5bits, G3 Gain adjustment: 8bits) to adjust the span voltage and another primary characteristics compensator for its associated temperature drift.

The output stage, with an internal resistor of 146kΩ, is band-limited with a combination of external capacitors, providing a low impedance output. And the EEPROM data, if used, enables the internal SCF and SMF. In this case, the band limitation is performed by the internal LPF (fc: 1kHz, 500Hz, 250Hz), eliminating the need for the external capacitors.

EEPROM data can be preconfigured to enable a setup of output reference voltage, designation of the external temperature sensor (when a pressure sensor and AK8998 are separated), selection of a sampling frequency (1kHz or 10kHz), the input polarity, and AGND pin validation.

Two sets of the pressure detectors are provided. When the pressure exceeding the detection threshold stored in the EEPROM is applied, the DET 1 and/or DET2/PTH pins go high (the polarity change is possible by EEPROM). And the detection threshold can be specified externally by EEPROM. In that case, the Pressure Detectors 2 is disabled, and the detection threshold for the Pressure Detectors 1 can be defined by DET2/PTH pin.

It can access to the EEPROM and control register (volatile memory) by a two-wire serial interface of CSCLK and VOUT (at the time of SDI/O mode) pin.

Pin Configuration

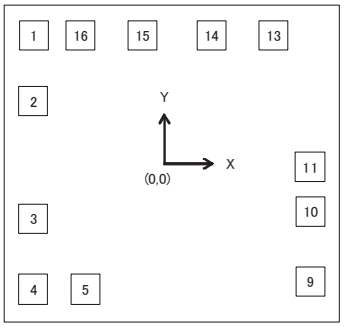
1. Wafer Configuration

1) Die size 2.082mm x 1.662mm
2) Die thickness 280μm
3) PAD size 80μm x 80μm
4) PAD pitch 150μm<
5) Scribe size 80μm
6) Wafer size 6 inch

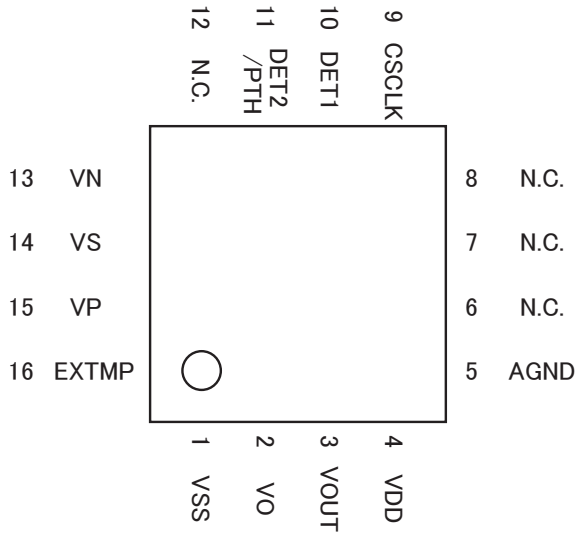
Pin numbers and Pad position

No.	Pin Name	X Location (μm)	Y Location (μm)	No.	Pin Name	X Location (μm)	Y Location (μm)
1	VSS	-894.8	687.2	9	CSCLK	894.8	-544.7
2	VO	-894.8	337.8	10	DET1	894.8	-242.5
3	VOUT	-894.8	-344.7	11	DET2/PTH	894.8	-57.9
4	VDD	-894.8	-687.1	12	N.C.		
5	AGND	-521.7	-684.8	13	VN	749.3	684.8
6	N.C.			14	VS	363.4	684.8
7	N.C.			15	VP	-236.7	684.8
8	N.C.			16	EXTMP	-716.4	684.8

Pad locations (Top view)



2. Package Outline (UQFN16)



Adjustment Characteristics

1) Sensor Characteristics

■VDD: 5V

Item	Symbol	Min.	Typ.	Max.	units	Comments
Drive voltage	Svs1		2.2		V	EVD[1:0]=1h
	Svs2		4.0		V	EVD[1:0]=0h
Temperature range	Sta	-20		85	°C	
Sensor resistance	Sres1	0.82	4.00	6.50	kΩ	EVD[1:0]=1h
	Sres2	1.00	4.00	6.50	kΩ	EVD[1:0]=0h
Voltage input span range	Sspnin1	12.00	44.00	76.00	mV	Sensor1
	Sspnin2	17.00	70.00	125.00	mV	Sensor2
Offset voltage adjustment range	Soff1	-15.00	0.00	15.00	mV	Sensor1
	Soff2	-35.00	0.00	35.00	mV	Sensor2
Sensitivity temp. drift coefficient	Sst1	-4000		2500	ppm/°C	ESTC[0]=1h
	Sst2	-2500		1000	ppm/°C	ESTC[0]=0h
Offset temp. drift coefficient	Sot1	-0.040	0.00	0.040	mV/°C	Sensor1
	Sot2	-0.080	0.00	0.080	mV/°C	Sensor2

■VDD:3, 3.3V

Item	Symbol	Min.	Typ.	Max.	units	Comments
Drive voltage	Svs		2.2		V	
Temperature range	Sta	-20		85	°C	
Sensor resistance	Sres	0.82	4.00	6.50	kΩ	
Voltage input span range	Sspnin1	6.60	24.20	41.80	mV	Sensor1
	Sspnin2	9.00	40.00	70.00	mV	Sensor2
Offset voltage adjustment range	Soff1	-8.25	0.00	8.25	mV	Sensor1
	Soff2	-19.25	0.00	19.25	mV	Sensor2
Sensitivity temp. drift coefficient	Sst1	-4000		2500	ppm/°C	ESTC[0]=1h
	Sst2	-2500		1000	ppm/°C	ESTC[0]=0h
Offset temp. drift coefficient	Sot1	-0.022	0.00	0.022	mV/°C	Sensor1
	Sot2	-0.044	0.00	0.044	mV/°C	Sensor2

Note) The usage combines characteristics of senser 1/2 is not allowed. Such a case as Span voltage is said as the sensor 1 and except is said as the sensor 2).

2) Adjustment Accuracy

Item	Symbol	Min.	Typ. Note4)	Max. Note5)	units	Comments
Offset adjustment accuracy	Cof		0.083		%FS	
Offset temp. drift adjustment accuracy	Coft		0.090		%FS	
Output span adjustment accuracy	Csn		0.125		%FS	
Sensitivity temp. adjustment accuracy	Csnt		0.054		%FS	
Sensitivity supply voltage and temp. variation step	Cstv		0.316		%FS	ESTC[0]=1h
			0.158		%FS	ESTC[0]=0h
Sample and hold circuit output error	Cshe		0.0		%FS	
Offset adjustment accuracy Note1)	Cofall		0.122	1.0	%FS	
Span adjustment accuracy Note2)	Csnall		0.344	1.0	%FS	ESTC[0]=1h
			0.209	1.0	%FS	ESTC[0]=0h
Offset adjustment accuracy Note3)	Call		0.344	1.0	%FS	ESTC[0]=1h
			0.209	1.0	%FS	ESTC[0]=0h

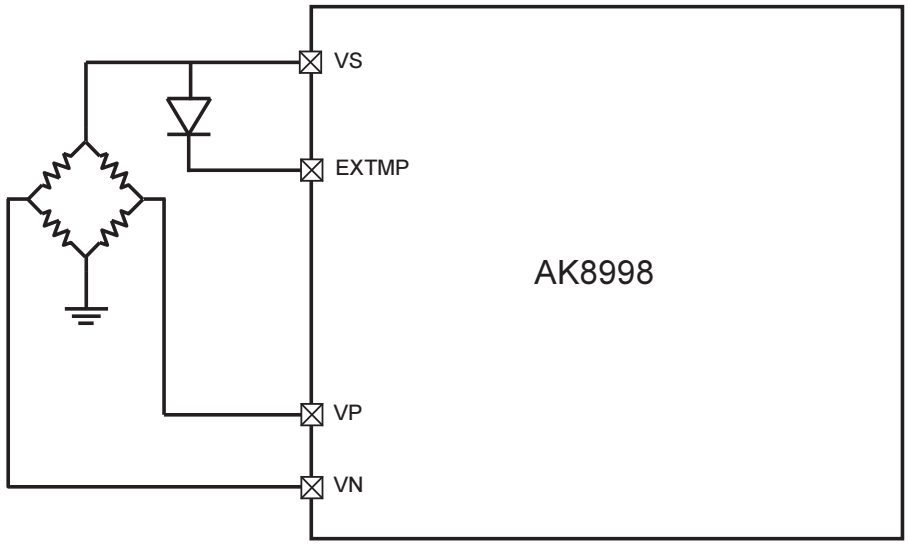
Note1) Cofall=(Cof^2+Coft^2)^(1/2)
Note2) Csnall=(Csn^2+Csnt^2+Cstv^2+Cshe^2)^(1/2)
Note3) Call=max(Cofall,Csnall)
Note4) Temp.=85ºC, VDD=4.75V, G1=10x, G2=1.5x(1.176x), G3=1.8x(2.3x), Offset temp. drift 1st order coefficient=Min./Max., Sensitivity temp. drift 1st order coefficient=Min.*1/2, VOUT output band-limited (≤500Hz @Fs=10kHz, ≤50Hz@Fs=1kHz) effective
Note5) Temp.=-20 to 85ºC, VDD=5V±5%, 3.3V±5%, 3.0V±5%, G1/G2/G3 =Min. to Max., Each temperature coefficient=Min. to Max., VOUT output band-limited (≤500Hz @Fs=10kHz, ≤50Hz@Fs=1kHz) effective

* The adjustment accuracy is based on our definition as a reference. Please be aware the accuracy of product depends on the sensor characteristics and adjustment method.

3) External Temperature Sensor Characteristics

Item	Symbol	Min.	Typ.	Max.	units	Comments
Sensor drive current	Tsdi		50		μA	
Sensor temp. variation	Tss	-2.4	-2.2	-2.0	mV/°C	50μA current drive
Sensor voltage @25°C	Tsv25	550	600	650	mV	50μA current drive

4) Connection of Pressure Sensor and External Temperature Sensor



Description of Blocks

[Gain Amplifier Block, LPF, S/H&SCF& Level shifter, Buffer&SMF]

The set of these blocks amplifies, compensates and outputs the pressure sensor level
This set of blocks intermittently amplifies, compensates, samples and holds the pressure sensor output. The output stage, with an internal resistor of 146kΩ, is band-limited with a combination of external capacitors, providing a low impedance output. SCF and SMF are available for output, eliminating the need for the external capacitors. A percentage designator is used, benchmarked with 4800mVdc output at 100%, reflecting the 60x increase in differential input from 80mVdc.

Block	Functions
Gain Amp. 1/2/3 Gain (G1/2/3)	Gain Amp.1 is a low-noise high-gain amplifier at the front end. The differential signal is amplified by a factor of 10x typ. (5x to 70x). Gain Amp.2 converts the G1 differential output to single-ended with reference to AGND and amplifies by a factor of 1.5x typ. (1.5x or 3.0x) or 1.176x typ. (1.176x or 2.352x). Gain Amp.3 amplifies by a factor of 1.8x typ. (1.1x to 1.8x) or 2.3x typ. (1.4x to 2.3x). G2 gain and G3 gain are changed automatically by sensitivity temperature drift adjustment range change setup (ESTC [0]). Span voltage is adjusted with G1/2/3 Gain (G1/2: rough adjustment, G3: fine adjustment).
Offset_Temp. Offset Offset Temp. track (G2)	The preloaded compensation data in the EEPROM enables the pressure sensor offset voltage and offset temperature drift to be compensated. The following adjustment value is AK8998 input conversion @5.0V. Offset adj.Adj. range Rough ±13 to ±373mV / Fine ±1 to ±34mV Adj. step Rough 2 to 53mV /step / Fine 0.01 to 0.27mV /step Offset temp. drift. adj. Adj. range ±0.04 to ±1.23mV/ ºC Adj. step 0.2 to 4.8µV/ºC step
STV VDD track Gain_Temp. (STV)	Supply voltage and sensitivity temperature variation compensation circuit. Monitors the AGND voltage to calculate the magnitude of supply voltage variation; the pressure sensor sensitivity temperature drift is calculated for entry into G3 using the temperature sensor output voltage and preloaded compensation data (EEPROM data). The sensitivity temperature drift adjustment range can be changed by EEPROM data (ESTC[0]). Sensitivity temp. drift. adj. Adj. range -4000ppm/ ºC to +2500ppm/ ºC or -2500ppm/ ºC to +1000ppm/ ºC Adj. step 18ppm/ ºC step
LPF	Anti-aliasing filter to eliminate the fold-back noise generated in the sample-and-hold circuit (S/H) in the later stage. The cutoff frequency is fc=60kHz.
S/H & Level Shift & SCF	S/H doubles the LPF output and samples and holds it. The output reference voltage can be changed. Output reference voltage adj. Adj. range 0.02*VDD to 0.98*VD Adj. step 0.002*VDD /step SCF is a low-pass filter used for internal band limiting without using the external capacitors. The cutoff frequency (fc: 1kHz /500Hz /250Hz) of the filter can be set by EEPROM.
Buffer & SMF	Buffer to produce a band-limited output with low impedance. Provides 1.111x output. 146kΩ internal resistance and an external capacitor (C) make the LPF characteristics. Change the external capacitance value according to the desired signal band for detection using the following equation: fc=1/(2*π* 146kΩ*C) (Hz) SMF is a low-pass filter (fc=10kHz) used for eliminating the clock noise produced by the SCF in the previous stage. SMF is switched on or off in combination with the previous-stage SCF using the EEPROM data.

Block	Functions
Timing Logic	Generates timing sync signals for internal operation and sampling frequencies for sensor output signals. Sampling frequency (fs): 10kHz or 1kHz
Regulator	Constant voltage generator circuit to drive the sensor. The drive voltage can be selected from the EEPROM depending on the supply voltage being used. Drive voltage: 2.2V @VDD:3, 3.3V±5%, 4.0/2.2V @VDD:5V±5%
Pressure Detector1, 2	Two sets of pressure detection circuits. The pressure range can be individually selected depending on the EEPROM data for the pressure detector. • Pressure above a certain value is detected • Pressure below a certain value is detected The DET1 and DET2/PTH pins go high when the detected pressure exceeds the threshold (the polarity change by EEPROM is possible). The detection threshold can be set by the input of DET2/PTH pin (when only pressure detector 1 is used) or using the EEPROM data in the AK8998. The hysteresis voltage can be adjusted at 2 bits (4 steps), and it varies ratiometrically with respect to the supply voltage as well as the detection threshold. Note that the exact pressure determination cannot be achieved until the VOUT pin output is stabilized at the time of power up or due to the above setup and buffer circuit feedback resistor and external capacitor values.

Reference Section & Others

Block	Functions
V_Bandgap (VBG) V_Reference (VREF) I_Reference (IREF)	Generates the reference voltage or bias current required for each circuit. Adjust the VREF voltage so that it is equivalent to 1.0V. VREF voltage adj. Resolution 3bits Adj. step 1% / step IREF current should be adjusted to 1.0V voltage across 1MΩ external resistor tied to VOUT pin. IREF current adj. Resolution 4bits Adj. step 2.8% / step
Oscillator (OSC)	Oscillator to generate timing sync signals for internal operation and sampling frequencies for sensor output signals. Oscillation frequency is adjusted as the counter result reaches the expected value, the internal counter counts for the period of CSCLK is high (2msec typ.). For the detail, refer to the Functional Description **1) Adjustment Procedure Description (Example)**. OSC adj. Resolution 4bits Adj. step 5% / step
V_temp. (VTMP)	Temperature sensor for converting the ambient temperature to voltage. Adjust the temperature sensor output voltage (VTMP voltage) so that it is equivalent to VREF voltage at 25ºC. And it is also possible to select the external temperature sensor by EEPROM in consideration of the case where a pressure sensor and the AK8998 are separated physically. When the external temperature sensor is chosen, the constant current of 50μA is sinked from the EXTMP pin to VSS. VTMP voltage adj.(internal) Resolution 6bits Adj. step 0.2% / step VTMP voltage adj.(external) Resolution 9bits (Rough/Fine=3/6bits) Adj. step Rough 10% /step / Fine 0.2% /step
V_Common (VCOM)	Generates analog circuit reference voltage 1/2VDD. The internal power-up circuit causes it to start up within the settling time for stable analog operation (Start Up valid time). AGND pin can be validated by EEPROM (EAGND[0]=1h). It is effective to improve the noise characteristic (See recommended connection examples for components). In the case of EAGND[0]=0h, the AGND pin is Hi-Z.
Power ON Reset(POR)	Power Up circuit is for stable analog operation upon power-up. In order to make the power-on reset effective, be sure to power up the supply voltage from below 0.1*VDD.
Serial I/F	Serial interface for accessing EEPROM and control register (volatile memory). It accesses using the CSCLK pin and the VOUT pin.
EEPROM & Control Register	EEPROM and control register (volatile memory). Used to store compensation values and measurement modes and to set up the measurement modes for adjustment.

Pin Assignments and Functions

PAD	Name	I/O	C load max.	R load min.	Type	Comments
1	VSS				GND	
2	VO	I			Analog	Resistive load connection prohibited ESCF[1:0]: Open when 1,2,3h
3	VOUT	O	50pF	9.5kΩ	Analog	Resistance load is connectable with VDD or VSS
		I/O	100pF		CMOS	Pull-down resistor (100kΩ) included when SDI/O mode
		O	300pF		Analog	Adjustment mode
4	VDD				Power	
5	AGND	O			Analog	EAGND[0]: Resistive load connection prohibited when 1h EAGND[0]: Open when 0h
6,7,8	N.C.					Do not connect
9	CSCLK	I			CMOS	Pull-down resistor (100kΩ) included
10	DET1	O			CMOS	
11	DET2 /PTH	O			CMOS	
		I			Analog	EPTH1[0]=1h
12	N.C.					Do not connect
13	VN	I			Analog	
14	VS	O	30pF	1kΩ	Analog	EVD[1:0]=0h
		O	30pF	0.82kΩ	Analog	EVD[1:0]=1, 2, 3h
15	VP	I			Analog	
16	EXTMP	I			Analog	Do not connect when not in use

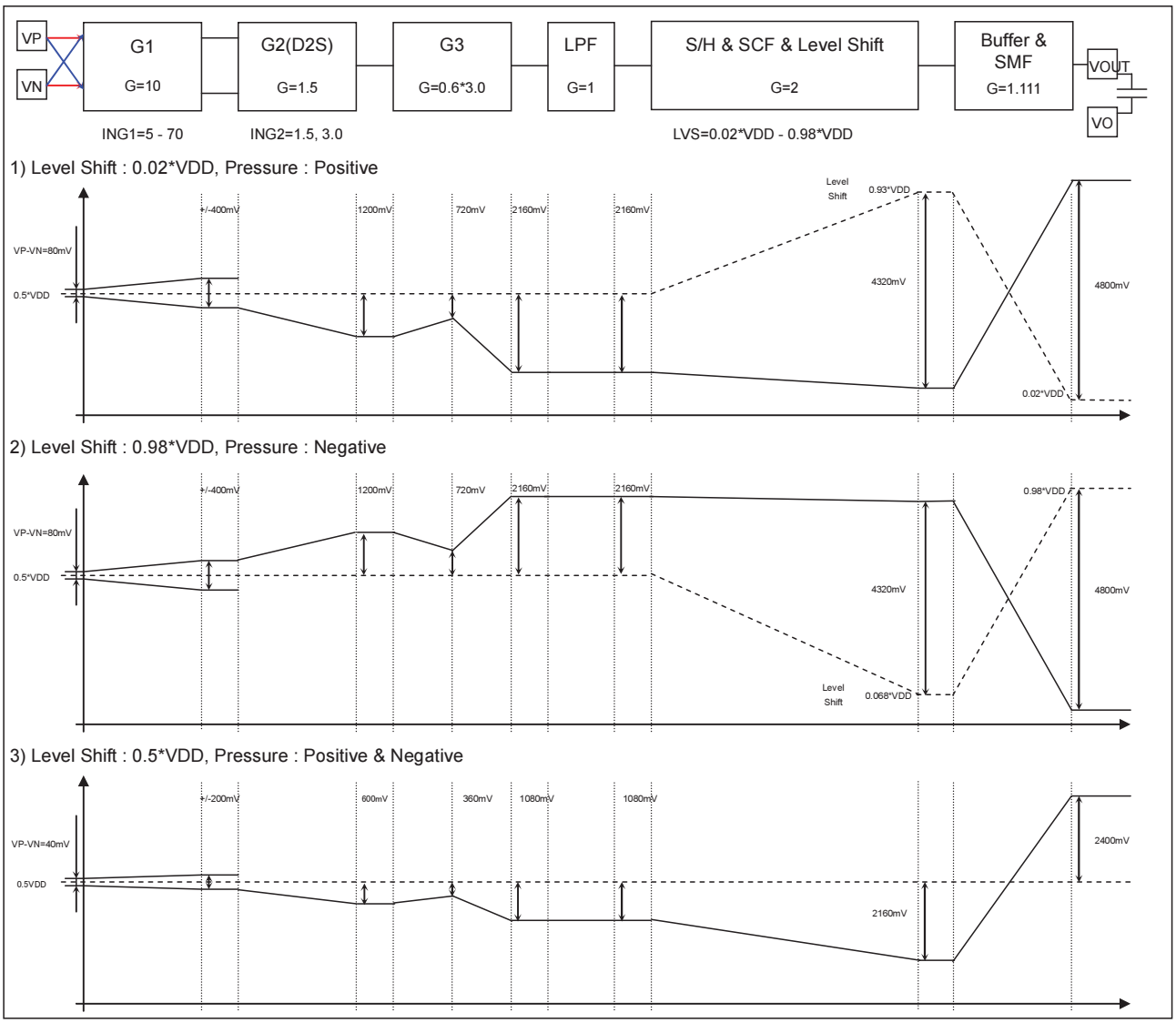
Pin Descriptions

PAD	Name	Functions	Pin conditions			
			Start up Note)	EAGND[0] : "H" / "L"	EINV1/2[0] : "H" / "L"	EINE1/2[0] : "H"
1	VSS	Negative voltage supply pin	-	-	-	-
2	VO	Capacitance connection pin for sensor signal band-limiting	Hi-Z	-	Normal operation	-
3	VOUT	Sensor signal / Data I/O / Calibration interface pin	Hi-Z	-	Normal operation	-
4	VDD	Positive supply voltage pin	-	-	-	-
5	AGND	Analog ground with external capacitance for stabilization	0.5*VDD /Hi-z	0.5*VDD /Hi-z	Normal operation	-
6,7,8	N.C.		-	-	-	-
9	CSCLK	Chip select / Serial clock pin	-	-	-	-
10	DET1	Output pin for pressure detection 1	VDD/VSS	-	VSS/VDD	VSS
11	DET2 /PTH	Output pin for pressure detection 2 / Pressure detection circuit 1 threshold external input	VDD/VSS	-	VSS/VDD	VSS
12	N.C.		-	-	-	-
13	VN	Sensor differential signal input pin (-)	-	-	-	-
14	VS	Constant voltage supply pin for sensor drive	Hi-z	-	Normal operation	-
15	VP	Sensor differential signal input pin (+)	-	-	-	-
16	EXTMP	External temperature sensor voltage input pin	Hi-z	-	-	-

Note) In the case of EAGND[0]="H"/"L" and EINV1/2[0]="H"/"L"

Level Diagram

VDD: 5V (ESTC[0]=1h)



Electrical Characteristics

1) Absolute Maximum Ratings

Item	Symbol	Min.	Max.	units	Comments
Supply voltage	VDD	-0.3	6.5	V	
Input voltage	VDIN	VSS-0.3	VDD+0.3	V	
Input current	IIN	-10	10	mA	
Output current	IOUT	-10	10	mA	
Storage temp.	TST	-55	125	°C	EEPROM retention characteristics ≤85°C

Note) Operation at or beyond these limits may result in permanent damage to the device.

2) Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	units	Comments
Operating temp.	Ta	-20		85	°C	
Supply voltage	VDD1	2.85	3.0	3.15	V	EVD[1:0]=3h
	VDD2	3.135	3.3	3.465	V	EVD[1:0]=2h
	VDD3	4.75	5.0	5.25	V	EVD[1:0]=0h, 1h

3) Supply Voltage Current (See Functional Description)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units	Comments
Supply voltage current 1	IDD1		6000	7100	μA	VDD=5V,VS=4V,Fs=10kHz Note1)
Supply voltage current 2	IDD2		4000	5000	μA	VDD=3V,VS=2.2V,Fs=10kHz Note1)
Supply voltage current 3	IDD3		1300	2000	μA	VDD=5V,VS=4V,Fs=1kHz Note1)
Supply voltage current 4	IDD4		1100	1700	μA	VDD=3V,VS=2.2V,Fs=1kHz Note1)
Supply voltage current 5 (SCF & SMF circuit)	IDD5		100	150	μA	VDD=5V
Supply voltage current 6 (Pressure detection circuit 1/2)	IDD6		150	250	μA	VDD=5V
Supply voltage current 7 (External temperature sensor drive circuit)	IDD7		130	200	μA	VDD=5V

Note) At the time of measurement, the VS pin connects 1kΩ load, the VOUT pin is connects no load, and the VP and VN pins supply 0.5*VS.
VREF and VTMP voltage, IREF current and OSC frequency are complete with adjustment.
Note1) SCF&SMFcircuit:Off, External temperature sensor drive circuit:Off

4) EEPROM Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units
EEPROM endurance	Etime	1000			times
EEPROM data retention time	Ehold	10			years

5) Digital DC Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	units
High level input voltage	VIH	1		0.7*VDD	-	-	V
Low level input voltage	VIL	1		-	-	0.3*VDD	V
High level input current	IIH	1		+10	-	+200	µA
Low level input current 1	IIL1	2		-10	-	+10	µA
Low level input current 2	IIL2	3		-50	-	+50	µA
High level output voltage	VOH	4	IOH=-200µA	0.9*VDD	-	-	V
Low level output voltage	VOL	4	IOL=+200µA	-	-	0.1*VDD	V

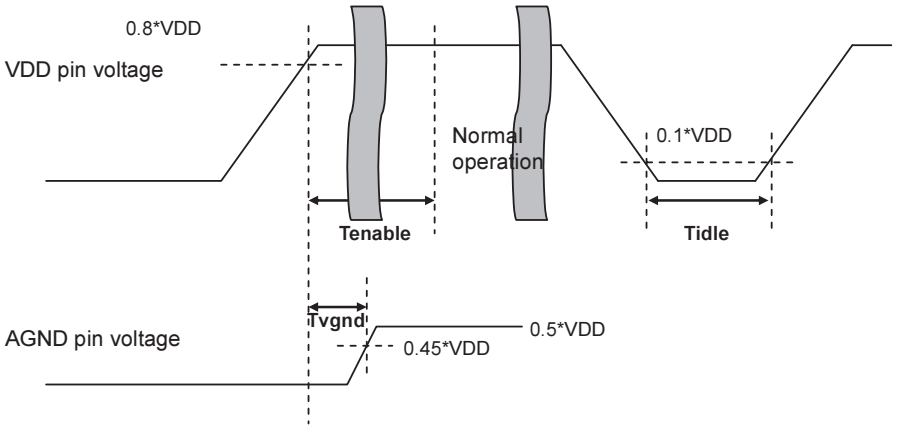
1 CSCLK(integrated 100kΩ pull-down resistor),
VOUT(integrated 100kΩ pull-down resistor when SDI/O mode)
2 CSCLK(integrated 100kΩ pull-down resistor),
3 VOUT(integrated 100kΩ pull-down resistor when SDI/O mode)
4 VOUT(when SDI/O mode), DET1, DET2/PTH

6) Power On/Off time and Analog circuit settling time for stable operation Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units	Comments
Power On/Off time	Tidle	10			msec	VDD pin voltage <0.1*VDD
Settling time for stable analog operation	Tenable			700	µsec	
AGND output rise time	Tvgnd			330	µsec	EAGND[0]=1h, AGND pin external capacitance: 10nF

Note) Design reference value; no production test performed.



7) Digital AC Characteristics

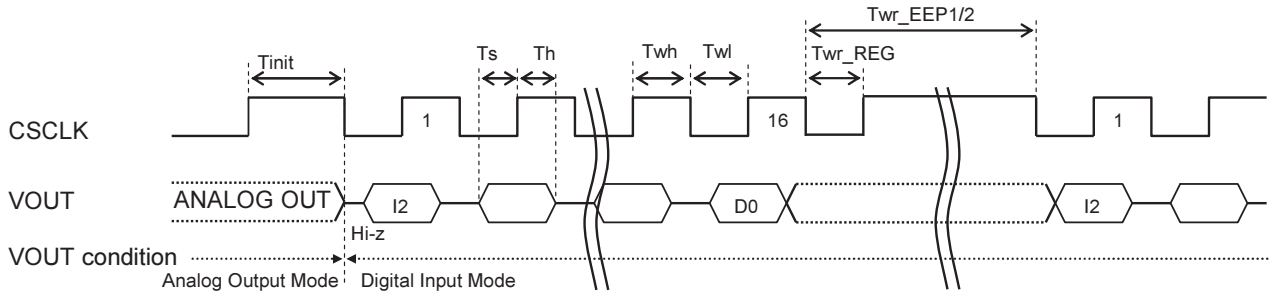
VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units
Write time (EEPROM address write)	Twr_EEP1	5		100	msec
Write time (EEPROM batch write)	Twr_EEP1	10		100	msec
Write time (Register)	Twr_REG	10			µsec
Digital Mode Transition time	Tinit	1.0			msec
Analog Mode Transition time	Tdigout	0.5			msec
Data setup time	Ts	100			nsec
Data hold time	Th	100			nsec
CSCLK high time	Twh	0.5		100	µsec
CSCLK low time	Twl	0.5		100	µsec
CSCLK→DO delay time Note1)	Td			200	nsec
CSCLK rising time Note 2)	Tr			10	nsec
CSCLK falling time Note 2)	Tf			10	nsec

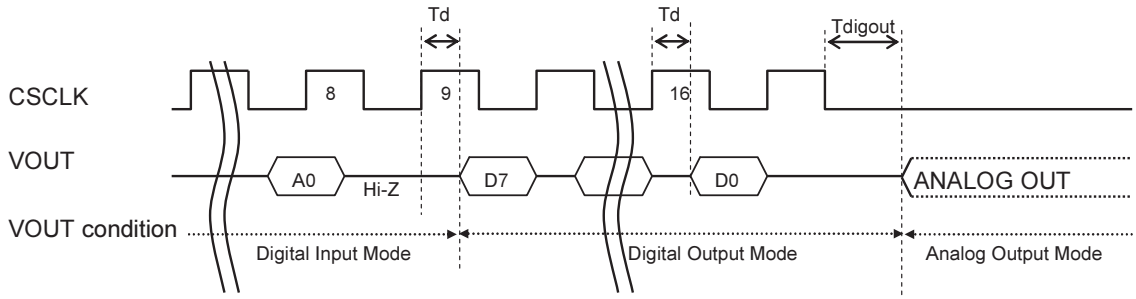
Note1) SDO load capacitance=100pF

Note2) Design reference value; no production test performed.

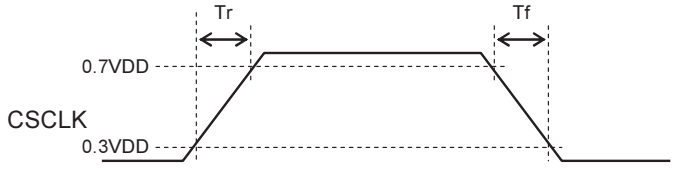
[Serial I/F timing (Write)]



[Serial I/F timing (Read)]



[CSCLK Raising/Falling timing]

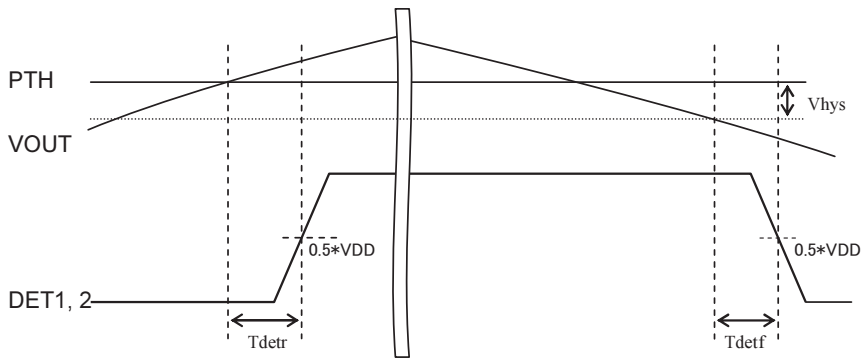


8) Pressure Detector 1 & 2

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Pressure detection threshold External input range	Vdete	EINE1[0]=0h EINE2[0]=1h EPTH1[0]=1h	0.1*VDD		0.9*VDD	V	
Pressure detection threshold Internal set value	Vdet	EPT1, 2[4:0]=00h	0.500 *VDD -0.05	0.500 *VDD	0.500 *VDD +0.05	V	
Pressure detection threshold Internal set value Adjust. width	Vdet+	Max: EPT1, 2[4:0]=10h		0.900 *VDD		V	
	Vdet-	Min: EPT1, 2[4:0]=0Fh		0.125 *VDD		V	
Adjust. step	Vdstp			0.025 *VDD		V	
Hysteresis voltage Adjust. width	Vhys5+	Max: VDD=5V±5% EHYS1, 2[1:0]=01h	0.060 *VDD -0.055	0.060 *VDD	0.060 *VDD +0.055	V	
	Vhys5-	Min: VDD=5V±5% EHYS1, 2[1:0]=10h	0.030 *VDD -0.03	0.030 *VDD	0.030 *VDD +0.03	V	
	Vhys3+	Max: VDD=3, 3.3V±5% EHYS1, 2[1:0]=01h	0.060 *VDD -0.035	0.060 *VDD	0.060 *VDD +0.035	V	
	Vhys3-	Min: VDD=3, 3.3V±5% EHYS1, 2[1:0]=10h	0.030 *VDD -0.02	0.030 *VDD	0.030 *VDD +0.02	V	
Adjust. step	Vhysst			0.010 *VDD		V	
Pressure detection time	Tdetr	ESCF[1:0]=0h			150	µsec	Note)
Pressure non-detection time	Tdetf	ESCF[1:0]=0h			150	µsec	Note)

Note) Design reference value; no production test performed.



9) Analog Characteristics
9-1) Reference Section

9-1-1) Reference Section Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
VREF voltage	Vr0	Unadjusted AM[3:0]=1h VOUT out	0.97	1.0	1.04	V	@25 ºC
VREF adj. width	Vr+	With respect to Vr0 Max EVR[2:0]=3h		+30		mV	
	Vr-	With respect to Vr0 Min EVR[2:0]=4h		-40		mV	
VREF adj. step	Vrstp			10		mV	
VS voltage	VS4	After VREF adj. VS pin out Load resistance 1kΩ	3.88	4.00	4.12	V	
	VS2	After VREF adj. VS pin out Load resistance 0.82kΩ	2.134	2.20	2.266	V	
IREF current	Ir0	Unadjusted AM[3:0]=2h VOUT out	0.8	1.00	1.2	μA	@25 ºC
IREF adj. width	Ir+	With respect to Ir0 Max EIR[3:0]=7h		0.24		μA	
	Ir-	With respect to Ir0 Min EIR[3:0]=8h		-0.17		μA	
IREF adj. step	Irstp			0.028		μA	
OSC freq.	Fr0	Unadjusted AM[3:0]=3h VOUT out	0.750	1.000	1.250	MHz	@25 ºC
OSC adj. width	Fr+	With respect to Fr0 Max EFR[3:0]=7h		384		kHz	
	Fr-	With respect to Fr0 Min EFR[3:0]=Bh		-251		kHz	
OSC adj. step	Frstp			50		kHz	
VTMP voltage	Vt0	Unadjusted ETMP[0]=1h AM[3:0]=4h VOUT out	0.938	1.0	1.064	V	@25 ºC
VTMP adj. width (Rough)	Vtr+	With respect to Vt0 ETMP[0]=0h Max ETM[8:6]=6h		+170		mV	
	Vtr-	With respect to Vt0 ETMP[0]=0h Min ETM[8:6]=2h		-170		mV	
Rough adj. step	Vtrstp	ETMP[0]=0h		85		mV	
VTMP adj. width (fine)	Vtf+	With respect to Vt0 ETMP[0]=1h Max ETM[5:0]=20h		+64		mV	
	Vtf-	With respect to Vt0 ETMP[0]=1h Min ETM[5:0]=1Fh		-62		mV	
Fine adj. step	Vtfstp	ETMP[0]=1h		2.0		mV	
VTMP temp variation	Vt	ETMP[0]=1h		4.6		mV/°C	Note)

Note) Design reference value; no production test performed.

9-1-2) Reference Section (packaged version only) Characteristics

VDD=5V±5%, Ta= 25ºC, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
VREF voltage	Vr0P		0.99	1.0	1.01	V	After adj.
VS voltage	VS4P	Load resistance 1kΩ	3.88	4.00	4.12	V	After adj.
	VS2P	Load resistance 0.82kΩ	2.134	2.20	2.266	V	After adj.
IREF current	Ir0P		0.9	1.0	1.1	μA	After adj.
OSC freq.	Fr0P		0.9	1.0	1.1	MHz	After adj.
VTMP voltage	Vt0P	ETMP[0]=1h	0.988	1.0	1.012	V	After adj.

Note) AK8998 is shipped with adjustment at VDD=5V&VS=4V (EVD[1:0]=0h) and internal temperature sensor use (ETMP[0]=1h). If VDD=5V&VS=2.2V (EVD[1:0]=1h), VDD=3.3V&VS=2.2V(EVD[1:0]=2h), VDD=3V&VS=2.2V(EVD[1:0]=3h) and external temperature sensor use (ETMP[0]=0h) are the actual operating condition, readjustment is required. Even if VDD=5V&VS=4V (EVD[1:0]=0h) and internal temperature sensor use (ETMP[0]=1h) are the operating condition, readjustment is recommended.

9-2) Gain Amplifier etc.

Unless otherwise specified, the following requirements apply.

- Reference Section is complete with adjustment.
- For supply voltage of 5V (3V), sensor drive voltage of 4V (2.2V), the level diagram includes G1 gain of 10x, G2 gain of 1.5x, G3 gain of 1.8x, Total gain of 60x, Level shift 0.02*VDD and the output voltage 4800mV (2400mV) is set as 100% based on a differential input of 80mV (40mV).

9-2-1) Overall Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Std. gain	Gtyp	VP/VN→VOUT		60		times	
Input common voltage	Vicom		0.45VS	0.5*VS	0.55VS	V	
Output common voltage	Vcom0	VP/VN→VOUT VP=VN=0.5*VS		0.5*VDD		V	
Max. output range	Vmax+	VP/VN→VOUT VP-VN=VSS or VDD	0.98 *VDD			V	
	Vmax-				0.02 *VDD	V	
Noise	Nout1	VP/VN→VOUT VP=VN=Open External feedback capacitance 2.2nF			260	μVrms	@1Hz - 100kHz Note)
	Nout2	VP/VN→VOUT VP=VN=Open ESCF[1:0]=1h			300	μVrms	@1Hz - 100kHz Note)

Note) Value for total gain of 180x (G1 gain: 30x, G2 gain: 1.5x, G3 gain: 1.8x, S/H gain: 2x, Buffer gain: 1.111x). Design reference value; no production test performed.

9-2-2) G1/2 Gain Adjustment Circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode							
Unadjusted G1/2 output voltage	Vg1	VP-VN=80mV VDD=5V±5%	1150	1200	1250	mV	
	Vg2	VP-VN=40mV VDD=3, 3.3±5%	550	600	650	mV	
G1 adjustment range	G1sc+	EIG[3:0]=Ch		5		times	
	G1sc-	EIG[3:0]=0h		70		times	
Adj. Step	G1stp			2,3,5,10		times	
G2 adj.	G2sc1+	EIG[4]=0h,ESTC[0]=1h		3		times	
	G2sc1-	EIG[4]=1h,ESTC[0]=1h		1.5		times	
	G2sc2+	EIG[4]=0h,ESTC[0]=0h		2.352		times	
	G2sc2-	EIG[4]=1h,ESTC[0]=0h		1.176		times	

9-2-3) Offset Voltage Adjustment Circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode							
Unadjusted output voltage	Vo01	VDD=3, 3.3, 5V±5%	0.5*VDD -0.10	0.5*VDD	0.5*VDD +0.10	V	
Offset rough adj. DAC adj. range	Ocr5+	EOCR[3]=0h EOCR[2:0]=7h VDD=5V±5%		+11200		mV	
	Ocr5-	EOCR[3]=1h EOCR[2:0]=7h VDD=5V±5%		-11200		mV	
	Ocr3+	EOCR[3]=0h EOCR[2:0]=7h VDD=3, 3.3±5%		+5600		mV	
	Ocr3-	EOCR[3]=1h EOCR[2:0]=7h VDD=3, 3.3±5%		-5600		mV	
Adj. step	Ocr5stp	VDD=5V±5%		1600		mV	
	Ocr3stp	VDD=3, 3.3±5%		800		mV	
Offset fine adj. DAC adj. range	Ocf5+	EOCF[7]=0h EOCF[6:0]=3Fh VDD=5V±5%		+1016		mV	
	Ocf5-	EOCF[7]=1h EOCF[6:0]=3Fh VDD=5V±5%		-1016		mV	
	Ocf3+	EOCF[7]=0h EOCF[6:0]=3Fh VDD=3, 3.3±5%		+508		mV	
	Ocf3-	EOCF[7]=1h EOCF[6:0]=3Fh VDD=3, 3.3±5%		-508		mV	
Adj. step	Ocf5stp	VDD=5V±5%		8		mV	
	Ocf3stp	VDD=3, 3.3±5%		4		mV	

9-2-4) Span Voltage Adjustment Circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage adjustment							
Unadjusted Span voltage	Vs01	VP-VN=80mV VDD=5V±5%	2010	2160	2310	mV	
	Vs02	VP-VN=40mV VDD=3, 3.3±5%	1005	1080	1155	mV	
Span adj. range	Sc+	ESC[7:0]=00h		100/100		times	
	Sc-	ESC[7:0]=FFh		100/163.75		times	
Adj. Step	Sc stp	N= 0 – +255		100/(100+0.25*N)		times	

9-2-5) Offset Temperature Drift & Sensitivity Temperature Drift Adjustment Circuit

9-2-5-1) Offset Temperature Drift Adjustment Circuit Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. Adj. range	DO5+	EOT[8]=0h EOT[7:0]=FFh VDD=5V±5%		+36.8		mV/°C	
	DO5-	EOT[8]=1h EOT [7:0]=FFh VDD=5V±5%		-36.8		mV/°C	
	DO3+	EOT[8]=0h EOT[7:0]=FFh VDD=3, 3.3±5%		+22.08		mV/°C	
	DO3-	EOT[8]=1h EOT[7:0]=FFh VDD=3, 3.3±5%		-22.08		mV/°C	
Adj. step	DO5 stp	VDD=5V±5%		0.144		mV/°C	
	DO3 stp	VDD=3, 3.3±5%		0.087		mV/°C	

Note) Design reference value; no production test performed.

9-2-5-2) Sensitivity Temperature Drift Adjustment Circuit Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. Adj. range	DS1+	ESTC[0]=1h,EST[8]=0h EST[7:0]=8Bh		+2500		ppm/°C	
	DS1-	ESTC[0]=1h,EST[8]=1h EST[7:0]=DEh		-4000		ppm/°C	
	DS2+	ESTC[0]=0h,EST[8]=0h EST[7:0]=38h		+1000		ppm/°C	
	DS2-	ESTC[0]=0h,EST[8]=1h EST[7:0]=8Bh		-2500		ppm/°C	
Adj. step	DS stp			18		ppm/°C	

Note) Design reference value; no production test performed.

9-2-6) Supply Voltage & Temperature Sensitivity Variation Adjustment Circuit (STV) Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Sensitivity variation characteristics 1 to supply voltage	SV1	SV circuit initial operation, ESTC[0]=1h			5.0	%	
	SV2	SV circuit 2nd operation, ESTC[0]=1h		±0.4		%	Based on SV1
Sensitivity variation characteristics 1 to operating temp.	ST1	ST circuit initial operation, ESTC[0]=1h			5.0	%	
	ST2	ST circuit 2nd operation, ESTC[0]=1h		±0.4		%	Based on ST1
Sensitivity variation characteristics 2 to supply voltage	SV3	SV circuit initial operation, ESTC[0]=0h			5.0	%	
	SV4	SV circuit 2nd operation, ESTC[0]=0h		±0.2		%	Based on SV3
Sensitivity variation characteristics 2 to operating temp.	ST3	ST circuit initial operation, ESTC[0]=0h			5.0	%	
	ST4	ST circuit 2nd operation, ESTC[0]=0h		±0.2		%	Based on ST3

9-2-7) LPF, S/H & Buffer

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
LPF freq. response	Fc1		40	60	80	kHz	
S/H&Buffer gain	SHG		1.935	2.222	2.523	times	
S/H&Buffer out pre-adj. error	SHerr		-65		65	mV	
BUF gain adj. width	Bufg		1.000	1.111	1.222	times	
VOUT output voltage range	Vbuf+	Load resistance 9.5kΩ (with VDD or VSS)	0.98 *VDD			V	
	Vbuf-				0.02 *VDD	V	
BUF feedback resistor value	Rbuf		102	146	190	kΩ	

9-2-8) Level shift

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Output reference voltage adj. width (Level shift)	Vlv+	Max ELV[8]=1h ELV[7:0]=FFh		1.00 *VDD		V	Note)
	Vlv-	Min ELV[8]=0h ELV[7:0]=FFh		0.00 *VDD		V	Note)
Adj. step	Vlstp			0.002 *VDD		V	

Note) It is limited to 0.98*VDD from 0.02*VDD by the VOUT output range.

9-2-9) SCF & SMF

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

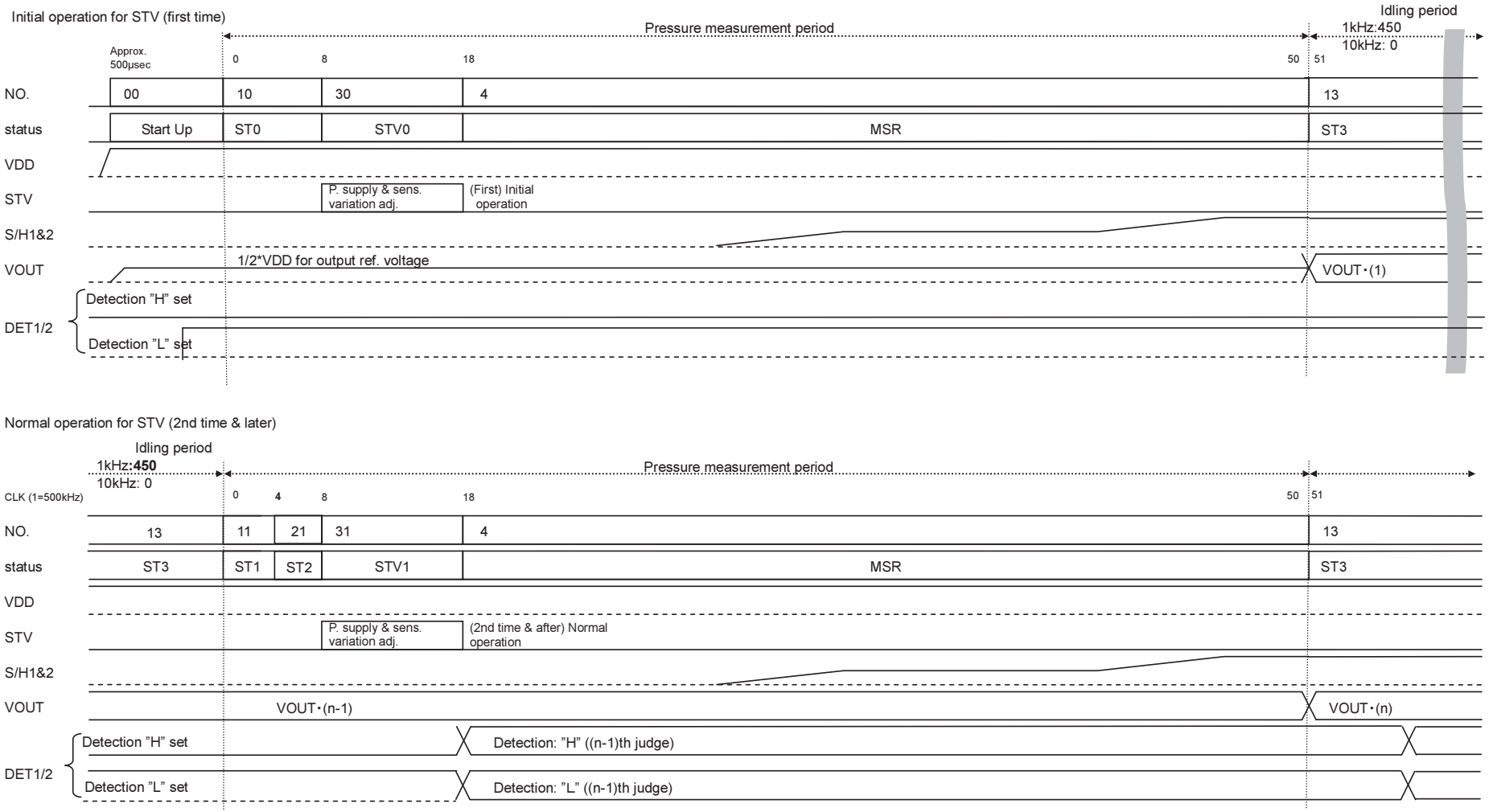
Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
SCF&SMF freq. response	Fc1	ESCF[1:0]=1h 10Hz referenced -3dB	0.8	1.0	1.2	kHz	
	Fc2	ESCF[1:0]=2h 10Hz referenced -3dB	400	500	600	Hz	
	Fc3	ESCF[1:0]=3h 10Hz referenced -3dB	200	250	300	Hz	
SCF&SMF gain	SCFG1	ESCF[1:0]=1h	1.000	1.111	1.222	times	

9-2-10) External temperature sensor drive circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Temperature sensor driving current	Iconst	After IREF adj.	40	50	60	µA	
Input voltage range	Extpv4	VS=4V After VREF adj.	3220	3400	3580	mV	
	Extpv2	VS=2.2V After VREF adj.	1474	1600	1726	mV	

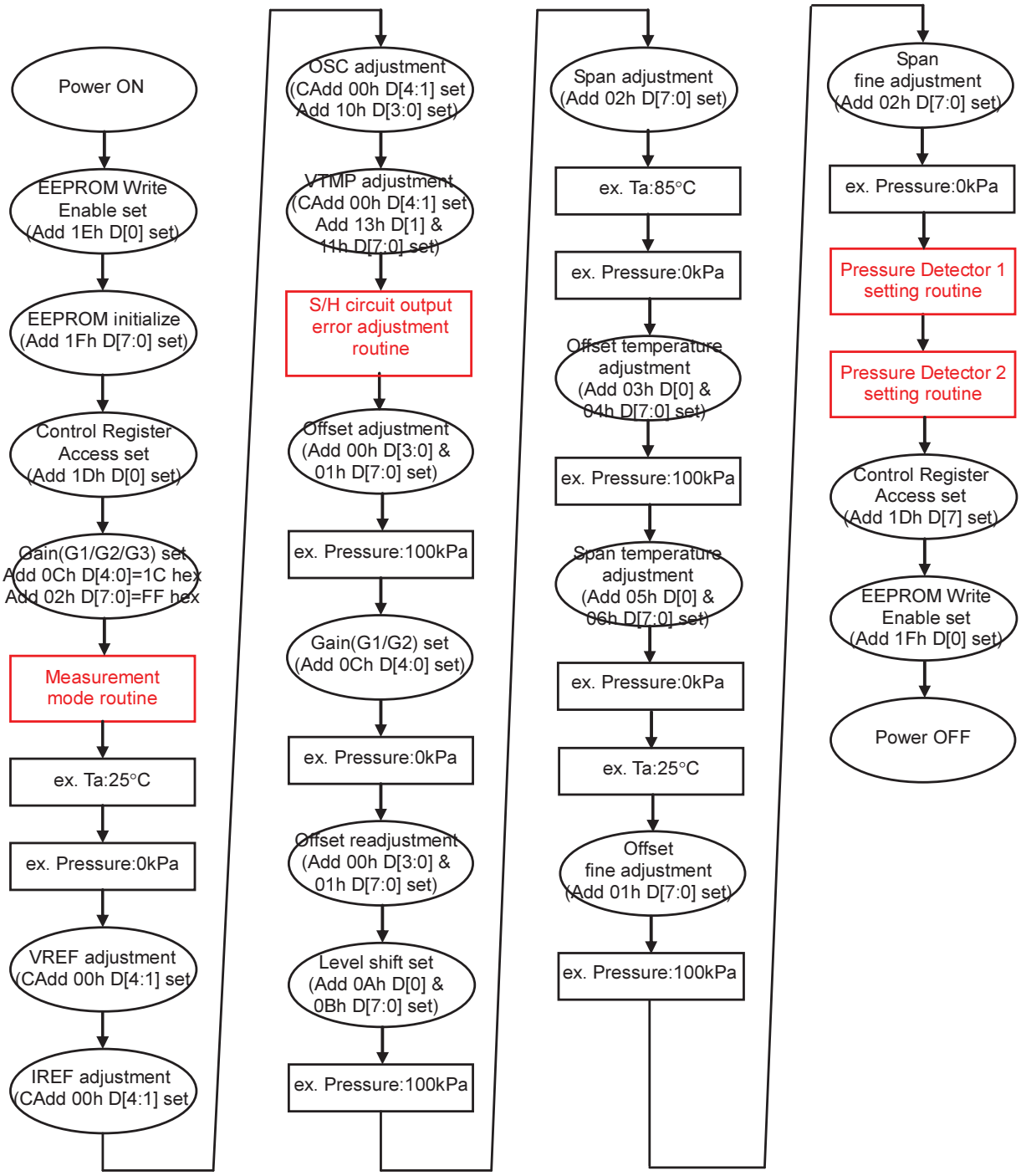
Operation Sequence



Description of Operation Timing Status (pressure detection circuit effective)

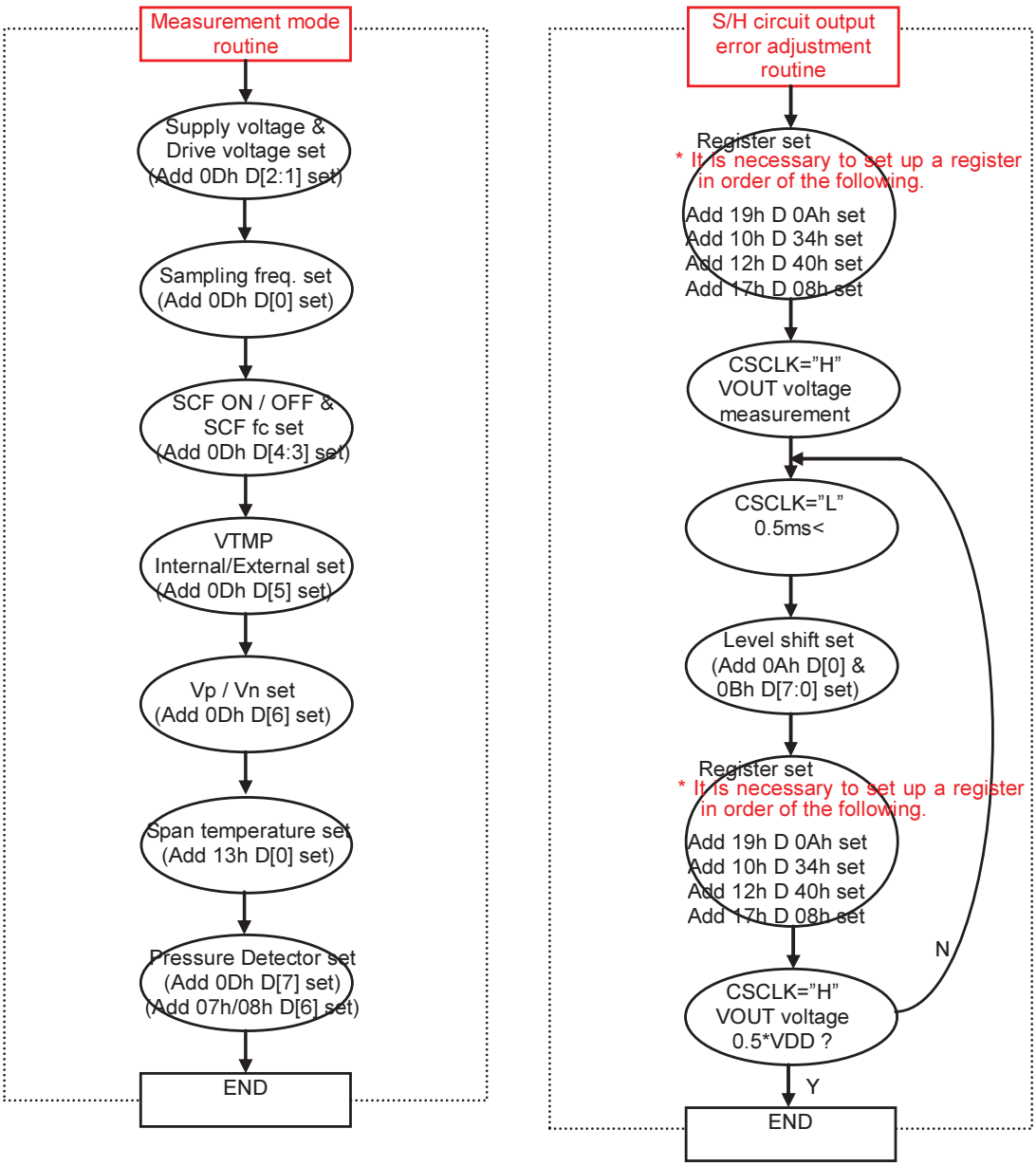
No.	State	CLK	Operations
00	Start Up		It is the time until analog circuits operate stably. Analog reference circuits as VREF, IREF, etc. start up and adjusted output reference voltage is output from the VOUT pin.
10	ST0		Clock count start Analog circuits startup
30	STV0	CLK=8	STV initial operation
4	MSR	CLK=18	The result of pressure correction is output from VOUT pin.
13	ST3	CLK=51	Idling With fs=10kHz, no idling and in continuous operation. Idling period 1kHz 450 CLK 10kHz 0 CLK
11	ST1	CLK1=51	Pressure detection circuit 1 operation and analog circuit startup
21	ST2	CLK=4+CLK1	Pressure detection circuit 2 operation
31	STV1	CLK=8+CLK1	STV normal operation Pressure detection DET1/2 output (the (n-1)th pressure determination)
:	:	:	:

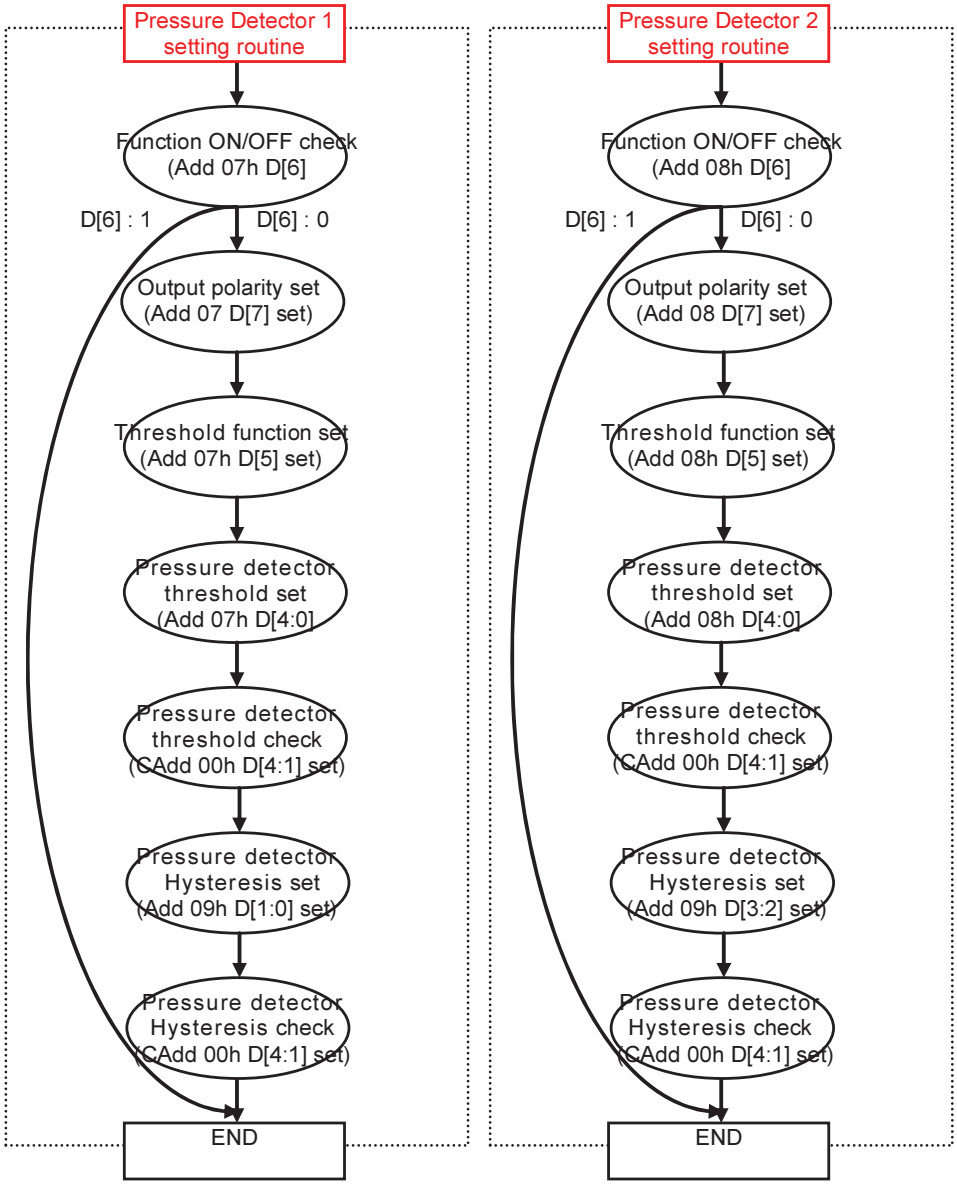
Adjustment Sequence



note1) EEPROM Address is indicated by “Add”,
Control Register Address is indicated by “CAdd”.

note2) Please refer the digital part flow chart
for EEPROM / Control Register writing and reading.


Measurement mode routine
Supply voltage & Drive voltage set (Add 0Dh D[2:1] set)
Sampling freq. set (Add 0Dh D[0] set)
SCF ON / OFF & SCF fc set (Add 0Dh D[4:3] set)
VTMP Internal/External set (Add 0Dh D[5] set)
Vp / Vn set (Add 0Dh D[6] set)
Span temperature set (Add 13h D[0] set)
Pressure Detector set (Add 0Dh D[7] set) (Add 07h/08h D[6] set)
END
S/H circuit output error adjustment routine
Register set
* It is necessary to set up a register in order of the following.
Add 19h D 0Ah set
Add 10h D 34h set
Add 12h D 40h set
Add 17h D 08h set
CSCLK="H" VOUT voltage measurement
CSCLK="L" 0.5ms<
Level shift set (Add 0Ah D[0] & 0Bh D[7:0] set)
Register set
* It is necessary to set up a register in order of the following.
Add 19h D 0Ah set
Add 10h D 34h set
Add 12h D 40h set
Add 17h D 08h set
CSCLK="H" VOUT voltage 0.5*VDD ?
N
Y
END


Pressure Detector 1 setting routine
Function ON/OFF check (Add 07h D[6]
D[6] : 1
D[6] : 0
Output polarity set (Add 07 D[7] set)
Threshold function set (Add 07h D[5] set)
Pressure detector threshold set (Add 07h D[4:0]
Pressure detector threshold check (CAdd 00h D[4:1] set)
Pressure detector Hysteresis set (Add 09h D[1:0] set)
Pressure detector Hysteresis check (CAdd 00h D[4:1] set)
END
Pressure Detector 2 setting routine
Function ON/OFF check (Add 08h D[6]
D[6] : 1
D[6] : 0
Output polarity set (Add 08 D[7] set)
Threshold function set (Add 08h D[5] set)
Pressure detector threshold set (Add 08h D[4:0]
Pressure detector threshold check (CAdd 00h D[4:1] set)
Pressure detector Hysteresis set (Add 09h D[3:2] set)
Pressure detector Hysteresis check (CAdd 00h D[4:1] set)
END

Functional Description

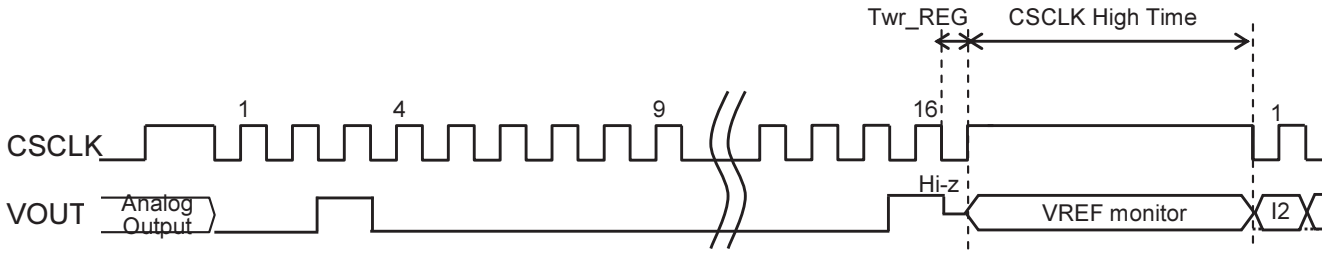
1) Adjustment Procedure Description (Example)

The adjustment procedure for the AK8998 follows (See "Adjustment Sequence.").

Note) When shipped in package form, the adjustments for the items 1-4 below have been completed. It is necessary to read the data (items 1-4 below) from a chip first and after initializing the EEPROM, rewrite the readout data. Note that depending on the required accuracy and implementation form, there could be some cases where items 1-4 should be readjusted.
AK8998 is shipped with adjustment at VDD=5V & VS=4V mode (EVD[1:0]=0h) and internal temperature sensor use (ETMP[0]=1h). If other modes (EVD[1:0]=1, 2, 3h, ETMP[0]=0h) are the actual operating condition, readjustment is required. Even if VDD=5V&VS=4V (EVD[1:0]=0h) and internal temperature sensor use (ETMP[0]=1h) are the operating condition, readjustment is recommended.
Keep the sequence as adjustment of VREF adjustment, IREF adjustment, OSC adjustment, and VTMP adjustment in turn. If VREF adjustment and IREF adjustment are performed after OSC adjustment, adjusted Oscillating frequency will shift.
The EEPROM address is referred to as "address," while the control register (volatile memory) address is referred to as "C address."

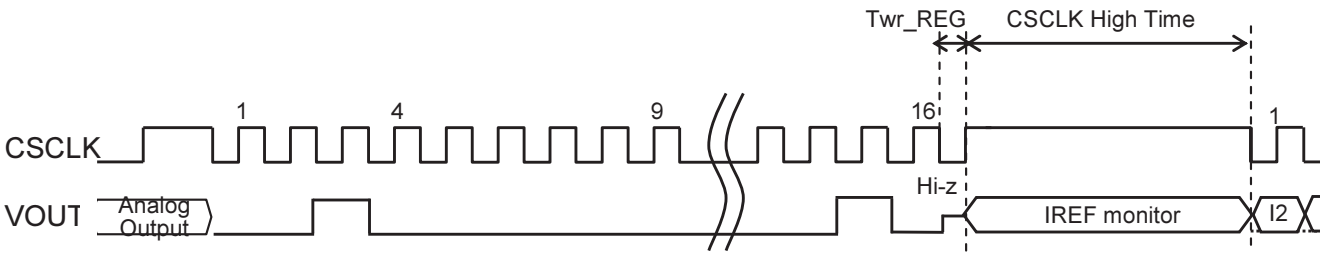
1. VREF Adjustment (completed when shipped in package form)

The reference voltage is adjusted to 1.0V by VREF voltage adjustment EEPROM (address: 0Eh, data EVR[2:0]). Adjusting the VREF voltage also means adjustment of the sensor drive voltage (VS). VREF voltage is observed at VOUT pin (See “Recommended Connection Examples for Components”) while the CSCLK pin High (CSCLK High Time) after the writing of an adjustment mode register (C address: 00h, data AM[3:0]= 1h).



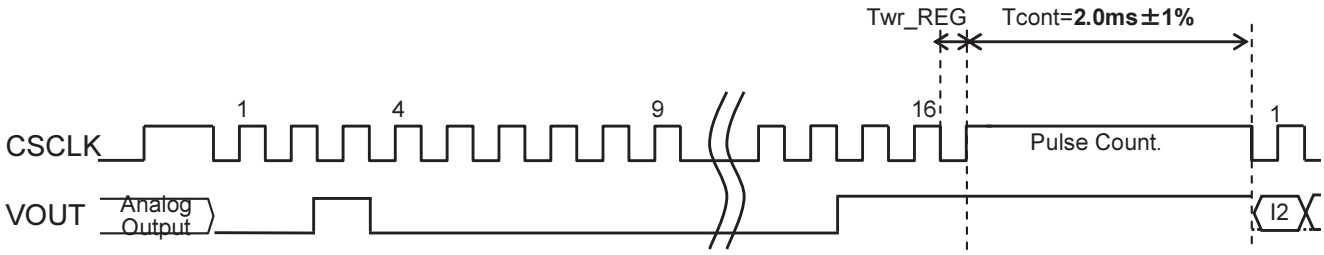
2. IREF Adjustment (completed when shipped in package form)

The reference current is adjusted to 1.0μA.
The external resistor (1MΩ) is connected to VOUT pin. Reference current is supplied to the external resistor, and IREF current adjustment EEPROM (address: 0Fh, data EIR[3:0]) is adjusted so that the voltage across the both ends of the external resistor is set to 1.0V. And it can adjust more accurate by taking into consideration the input impedance (input resistance) of adjustment apparatus. With 1MΩ external resistor to the VOUT pin, it is adjusted in voltage domain. The external 1MΩ should be connected only at the time of IREF adjustment. When with resistance 1MΩ is connected always in outside, please be careful of the input impedance of adjustment apparatus. The input impedance of adjustment apparatus should become more than 10GΩ. IREF current is observed at VOUT pin (See “Recommended Connection Examples for Components”) while the CSCLK pin High (CSCLK High Time) after the writing of an adjustment mode register (C address: 00h, data AM[3:0]= 2h).



3. OSC Adjustment (completed when shipped in package form)

The intermittent operation control clock is adjusted to 1,000kHz.
Oscillation frequency can be adjusted without monitoring frequency directly.
The high level for the fixed period (2.0msec±1%) is inputted from the CSCLK pin after the writing of an adjustment mode register (C address: 00h, data AM[3:0]= 3h). The internal clock pulses are counted in the integrated counter circuit, and the count value is stored in the control register (C address: 01h, data CT[7:0]). The adjustment data (address: 10h, data EFR[3:0]) for oscillation frequency is calculated from the stored count value. The adjustment can be done within 1000kHz±5% accuracy by writing the adjustment data in EEPROM. Since the error of High period turns into an adjustment error of frequency, please set period as 2.0ms±1%.



The explanation of oscillation frequency adjustment data (address: 10h, data EFR[3:0]) is as follows.

The count value stored in the control register (C address: 01h, data CT[7:0]) is read for the ratio check. A ratio will be 0% (ideal value), when the High level period of CSCLK pin is 2 msec and the frequency of the internal oscillator is 1000 kHz. The ratio varies from 0% by the error of High level period and the frequency variation of the internal oscillator. And the High time which can be set up becomes a range from which a ratio will be -99% to 154%. Be aware that the error is easily affected when the ratio is small. In addition, the counter value shown as FF hex means overflow, please measure again by changing High level period.

Please set the adjustment data of oscillation frequency as the sum of the ratio of CT [7:0] data and the ratio of EFR [3:0] data is close to 0%.

Address : 01 hex D[7:0]=CT[7:0]

CT[7:0]			Count value	Ratio	Comments
Dec	Hex	Bin	(time)	(%)	
0	00	00000000	0	0	Default
1	01	00000001	1	-99	
:	:	:	:	:	
98	62	01100010	98	-2	
99	63	01100011	99	-1	
100	64	01100100	100	0	Ideal value
101	65	01100101	101	1	
102	66	01100110	102	2	
:	:	:	:	:	
254	FE	11111110	254	154	
255	FF	11111111	-	-	Counter error

Address : 10 hex D[3:0]=EFR[3:0]

EFR[3:0]			Ratio	Frequency Δf	Comments
Dec	Hex	Bin	(%)	(kHz)	
-5	B	1011	-34	-251	
-4	C	1100	-25	-197	
-3	D	1101	-17	-146	
-2	E	1110	-11	-99	
-1	F	1111	-5	-52	
0	0	0000	0	0	Default
1	1	0001	5	49	
2	2	0010	10	106	
3	3	0011	14	162	
4	4	0100	18	224	
5	5	0101	22	274	
6	6	0110	25	329	
7	7	0111	28	384	

Note1) Hex 8 to A are prohibited for setup.

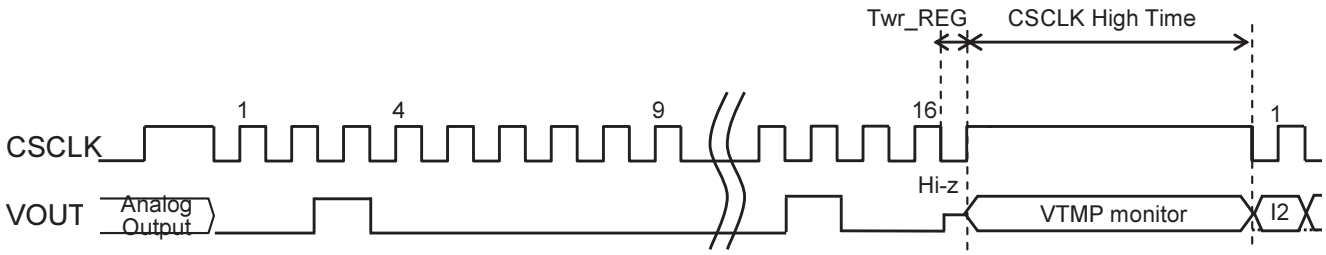
When High level period is not 2 msec, the ideal value of CT [7:0] can be calculated as follows.
Considering the calculated ideal value as 100%, and a ratio should be redefined. Please set the adjustment data of oscillation frequency as the sum of the ratio of CT [7:0] data and the ratio of EFR [3:0] data is close to 0%.

Count value[time]=High time[msec] / 2 * 100
ex.) In the case of 3 msec, 100 time → 150 time.

4. VTMP Adjustment (completed when shipped in package form)

Temperature sensor output (VTMP) voltage is adjusted to match the VREF voltage.
When the external temperature sensor is used, connect the external temperature sensor to the EXTMP pin, and set up a measurement mode EEPROM (address: 0Dh, data ETMP[0]= 0h).
VTMP voltage is observed at VOUT pin while the CSCLK pin High (CSCLK High Time) after the writing of an adjustment mode register (C address: 00h, data AM[3:0]= 4h).

*In sampling frequency 1kHz mode (ESF[0] =1h), the external temperature sensor (ETMP[0] =0h) cannot be used.



5. S/H Circuit Output Error Adjustment

The S/H circuit output voltage is adjusted to become 0.0V at VOUT pin by using the Output reference voltage adjustment EEPROM (address:0Ah data:ELV[8], address:0Bh data:ELV[7:0]).

6. Offset Voltage Adjustment

The offset voltage for the pressure sensor is adjusted including the AK8998 internal error by using the offset voltage adjustment EEPROM (address:00, 01h data:EOCR[3:0], EOCF[7:0]).

■Offset Voltage Adjustment Example (@VDD:5V)
EOCR[3]: Offset voltage rough adjustment sign bit
If unadjusted output is more than 0.5*VDD, set EOCR[3]=1h.
If unadjusted output is less than 0.5*VDD, set EOCR[3]=0h.
EOCR[2:0]: Offset voltage rough adjustment: Adjust in 1600-mV steps.
EOCF[7]: Offset voltage fine adjustment sign bit
If unadjusted output is more than 0.5*VDD, set EOCF[7]=1h.
If unadjusted output is less than 0.5*VDD, set EOCF[7]=0h.
EOCF[6:0]: Offset voltage fine adjustment: Adjust in 8-mV steps.

When the offset voltage is +360mV (0.5*VDD reference), set EOCF[7]=1h and EOCF[6:0]=45dec.
360[mV]-(8[mV]*45[dec])=0.0[mV]

7. Input gain (G1/G2) setup

Set up G1/G2 gain so that Gain Amp.1/2 output voltages become the ranges (In the case of VDD=5V, G1≤ 1700mV, G2≤ 1950mV). The voltage and temperature coefficient which are used for calculation is as follows.
The offset voltage and the span voltage in 25 °C are calculated by dividing the measurement result (VOUT pin) of the 1st offset voltage and the Span voltage by 18.35 (total gain). And for the offset voltage temperature drift coefficient and the sensitivity temperature drift coefficient, the MIN value (minus polarity) of the pressure sensor assumed is used.
In addition, since offset voltage and the offset voltage temperature drift coefficient are adjusted with Gain Amp.1 output, G2 gain is calculated noting that only the Span voltage and the sensitivity temperature drift coefficient.

Voff25: Offset voltage of the pressure sensor@25°C
Vsp25: Span voltage of the pressure sensor @25°C
Ktoff: Offset voltage temperature drift coefficient of the pressure sensor (MIN value)
Ktsp: Sensitivity temperature drift coefficient of the pressure sensor (MIN value)

■ In the case of VDD=5V and temperature=-20 to 85°C
Gain Amp.1 output
=G1*(Voff25+Vsp25+ktoff*(-20[°C]-25[°C])+Vsp25*ktsp*(-20[°C]-25[°C])) ≤ 1700mV
Gain Amp.2 output
=G1*G2*(Vsp25+Vsp25*ktsp*(-20[°C]-25[°C])) ≤ 2100mV

■ In the case of VDD=3.3V/3.0V and temperature=-20 to 85°C
Gain Amp.1 output
=G1*(Voff25+Vsp25+ktoff*(-20[°C]-25[°C])+Vsp25*ktsp*(-20[°C]-25[°C])) ≤ 800mV/800mV
Gain Amp.2 output
=G1*G2*(Vsp25+Vsp25*ktsp*(-20[°C]-25[°C])) ≤ 1250mV/1150mV

8. Offset Voltage Readjustment

The offset voltage is readjusted.
The offset voltage adjustment EEPROM is once reset to ALL"0", and the adjustment should be done again using the offset voltage adjustment EEPROM.

9. Output Reference Voltage Adjustment

Adjust the output reference voltage. The output reference voltage is adjusted by using the output reference voltage adjustment EEPROM (address: 0A, 0Bh data: ELV[8:0]).

■Output Reference Voltage Adjustment Example (@VDD:5V)

When the output reference voltage is 100mV, set ELV[8]=0h and ELV[7:0]=240dec.

2500[mV]+(-0.002*VDD*240[dec])*5000[mV]=100[mV]

10. Output Span Voltage Adjustment

The output span voltage for the connected pressure sensor is adjusted, including the AK8998 internal error, by using the output span voltage adjustment register (address: 02h data: ESC[7:0]).

■Output Span Voltage Adjustment Example (@VDD:5V)

When the output is 3700mV, set ESC[7:0]=140dec (target span voltage 4800mV).

(3700[mV]-100[mV])*1.8*100/(100+0.25*(140))=4800[mV]

11. Offset Temperature Drift Adjustment

The offset temperature drift for the pressure sensor is adjusted, including the AK8998 internal error, by using the offset voltage temperature drift adjustment register (address: 03, 04h data: EOT[8:0]).

■Offset Temperature Drift Adjustment Example (@VDD:5V)

EOT[8]: Offset voltage adjustment sign bit

If unadjusted output is greater than the output reference voltage, set EOT[8]=1h.

If unadjusted output is smaller than the output reference voltage, set EOT[8]=0h.

EOT[7:0]: Offset voltage adjustment: Adjust in 0.144mV/ºC steps (@VDD: 5V).

If the offset voltage is +300mV (with respect to the output reference voltage e.g.100mV) at Ta=85°C, set EOT[8]=1h, EOT[7:0]=35dec.

(100[mV]+300[mV])-(85[°C]-25[°C])*(0.144[mV/°C]*35[dec])=97.6[mV]

12. Sensitivity Temperature Drift Adjustment

The sensitivity temperature drift for the pressure sensor is adjusted, including the AK8998 internal error, by using the sensitivity temperature drift adjustment register (address: 05, 06h data: EST[8:0]).

■Sensitivity Temperature Drift Adjustment Example (@VDD:5V, ESTC[0]=1hex)

EST[8]: Sensitivity temperature drift adjustment sign bit (target span voltage 4800mV)

If unadjusted output is greater than 4800mV (with respect to the output reference voltage) at Ta=85°C, set EST[8]=1h.

If unadjusted output is smaller than 4800mV (with respect to the output reference voltage) at Ta=85°C, set EST[8]=0h.

EST[7:0]: Sensitivity temperature drift adjustment: Adjust in 18ppm/°C steps (@VDD: 5V).

If the output voltage is +4,400mV (with respect to the output reference voltage e.g.100mV) at Ta=85°C, set EST[8]=0h, EST[7:0]=77dec.

4400[mV])+(85[°C]-25[°C])*(18[ppm/°C]*77[dec])*4800[mV]=4799.2[mV]

13. Offset Voltage Fine Adjustment

The offset voltage error is caused by compensating the offset voltage temperature drift. The offset voltage is adjusted using the offset voltage fine adjustment EEPROM (Address: 01h data: EOCF[7:0]).

14. Output Span Voltage Fine Adjustment

The output span voltage error is caused by compensating the offset voltage temperature drift. The output span voltage is adjusted using the output span voltage adjustment register (Address: 02h data: ESC[7:0]).

2) Finding the VOUT and VO Pins External Capacitance (Cap)

This section explains how the VOUT and VO pins external capacitance is defined.
The requirements for determining the VOUT and VO pins external capacitance values are the stabilization time on power-up and S/(N+D)=Signal/(Noise+Distortion).

1. VOUT Pin Output Voltage Stabilization Time

Note that depending on the VOUT and VO pins external capacitance values, the measurement values (VOUT pin voltage) may contain errors upon power-up.

"99% Settling time (③+④ in the figure)" in the table below represents the analog stabilization time ③ in the figure and the time required to settle down to 99% of the output voltage (0.1*VDD in this case) according to the pressure applied during the period (③+④ in the figure).
The period ③ in the figure is 0.30msec (typ).
Subsequently, the output voltage will settle to 99% according to the pressure during period ④ in the figure. When the VO pin capacitance is 1μF, the period ④ in the figure will settle within 672.4msec.

Settling time (period ④ in the figure) =-146[kΩ]*1[μF]*ln(1-99/100)=672.4 [msec]

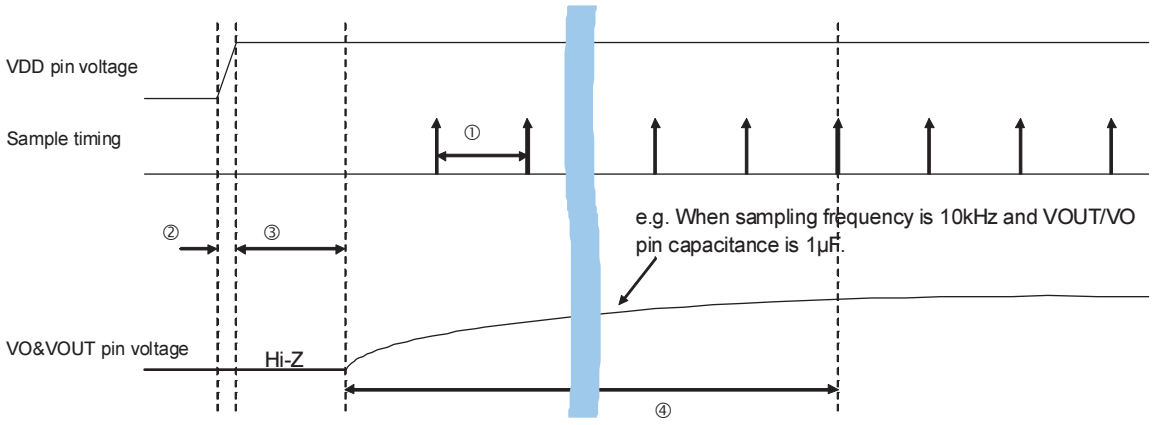
Therefore, the settling time up to 99% (period ③+④ in the figure) will be as follows:

99% settling time (period ③+④ in the figure) = 0.30[msec] + 672.4[msec] = 672.7 [msec]

Referring to the previous calculation example, determine the stabilization time based on true terms of use:

Prerequisites:	VO pin external capacitance:	Cap（Cap[μF] typ., Cap*1.1[μF] worst）
	VO pin internal resistance:	Res（146[kΩ] typ., 190[kΩ] worst）
	Period ③ in the figure:	Time（0.30[msec] typ., 0.40[msec] worst）

Settling time (period ④ in the figure) = -Res*Cap*ln(1-99/100)
99% settling time (period ③+④ in the figure) = Time + Settling time



① - ④ Reference designators
①: Sampling timing; this diagram represents 10kHz (0.1msec).
②: Power-up rise time (VDD).
③: Settling time for stable analog operation.
④: Pressure signal detection time. This time depends on the VO pin external capacitance and the internal 146kΩ resistance.

VO pin Ext. cap (nF)	Cutoff Freq.(Hz) (Typical)	Fig ③Time (msec)		99% Settling time (ms) (④)		99% Settling time (ms) (③+④)	
		Typical case	Worst case Note)	Typical case	Worst case Note)	Typical case	Worst case Note)
1000	1.090	0.300	0.400	672.4	962.5	672.7	962.9
220	4.955	0.300	0.400	147.9	211.7	148.2	212.1
22	49.55	0.300	0.400	14.79	21.17	15.09	21.57
2.2	495.5	0.300	0.400	1.479	2.117	1.779	2.517
0.22	4.96k	0.300	0.400	0.148	0.212	0.448	0.612
0.1	10.9k	0.300	0.400	0.067	0.096	0.367	0.496

Note) Worst case for external capacitance ±10% and lot variations.

2. VOUT pin S/(N+D)

Summarized in this table is the relationship between the VO pin's external capacitance and S/(N+D).
Note that the S/(N+D) should be 40dB or larger if 1.0% FS adjustment accuracy is required.

Sampling Freq.(Hz)	VO pin Ext. cap (nF)	Cutoff Freq.(Hz) (Typical)	S/(N+D) characteristics	
			Typical case	Worst case Note)
1	1000	1.090	68.8	64.6
	220	4.955	55.6	51.4
	22	49.55	35.6	31.4
	2.2	495.5	15.8	11.8
10	220	4.955	75.6	71.4
	22	49.55	55.6	51.4
	2.2	495.5	35.6	31.4
	0.22	4.96k	15.8	11.8

Note) Worst case for external capacitance ±10% and lot variations.

As mentioned in Sections "1. VOUT pin output voltage stabilization time" and "2. VOUT pin S/(N+D)", the VO pin external capacitance value should be reduced to decrease the measurement time. For increased S/(N+D), the VO pin external capacitance value should be greater.
On determining the VO pin external capacitance value, the various conditions should be thoroughly reviewed according to the application requirements.

3) Pressure Detection Operation at Power-Up

Use caution when operating the pressure detection circuits.
VOUT pin output voltage is settled down based on the time constant determined by the internal resistance 146kΩ and VO pin external capacitance Cap value (see 2) Finding the VO Pin External Capacitance (Cap)). Note that errors may be detected during the time in which VOUT pin output is not settled down to the voltage required according to the pressure applied.

4) Power Consumption

Current values described in 3) Supply Voltage Current in the Electrical Characteristics are those for the average current. The maximum current is shown in the table below. Use a power supply with sufficient supply capacity by referring to this table:

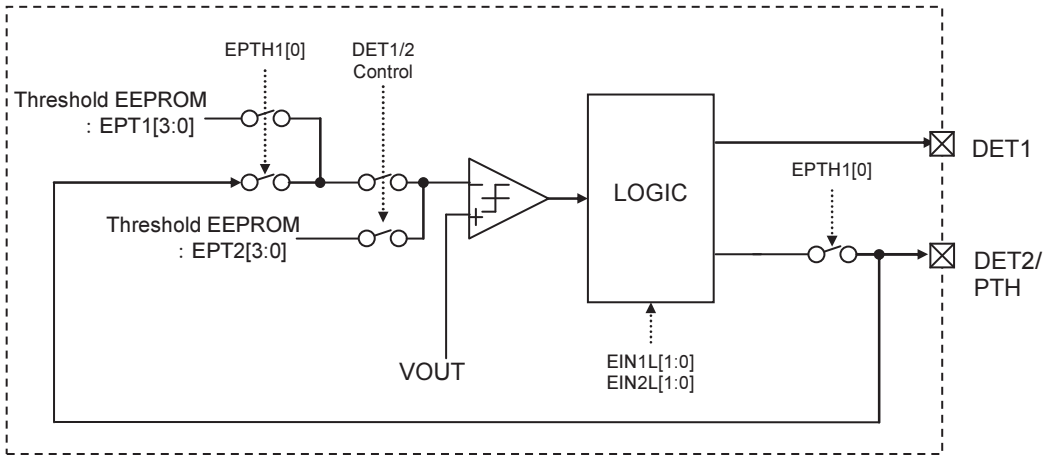
	units	VDD:3.6V	VDD:5.5V	Comments
Max. Current	mA	5.5	7.5	Reference value for design

5) Pressure Detectors 1 and 2

5-1) Pressure Detector's Detection Threshold

The internal setup and external setup for the pressure detectors' (1 and 2) detection threshold is described.

Block diagram of the pressure detectors 1 and 2:



The detection threshold of the pressure detectors 1 and 2 can be set up, as shown in the block diagram. For the pressure detectors 1 either through the external input (DET/PTH pin) or internal setup (EEPROM setup EPT1[4:0]) is used, for the pressure detector 2 only the internal setup (EEPROM setup EPT2[4:0]) is used.

5-2) Pressure Detector's hysteresis voltage

The hysteresis voltage in the pressure detectors' (1 and 2) detection threshold is described.

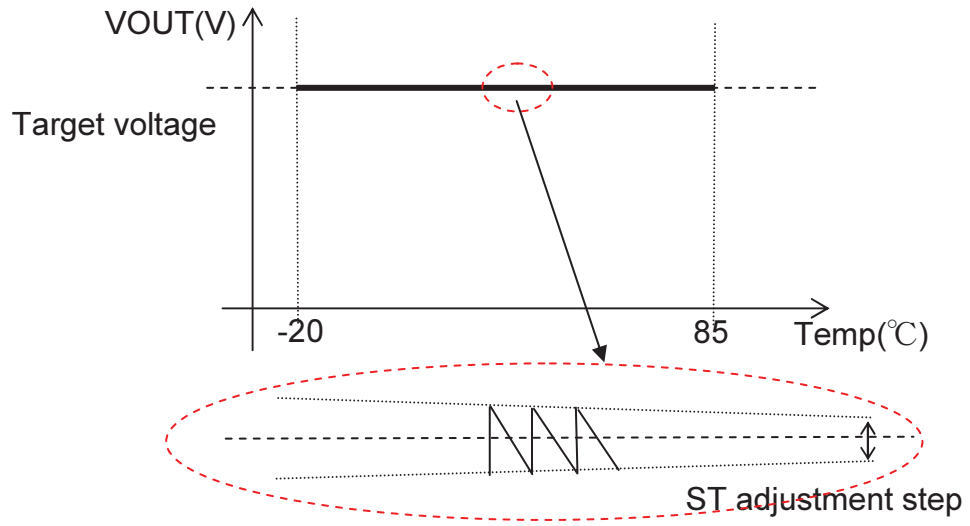
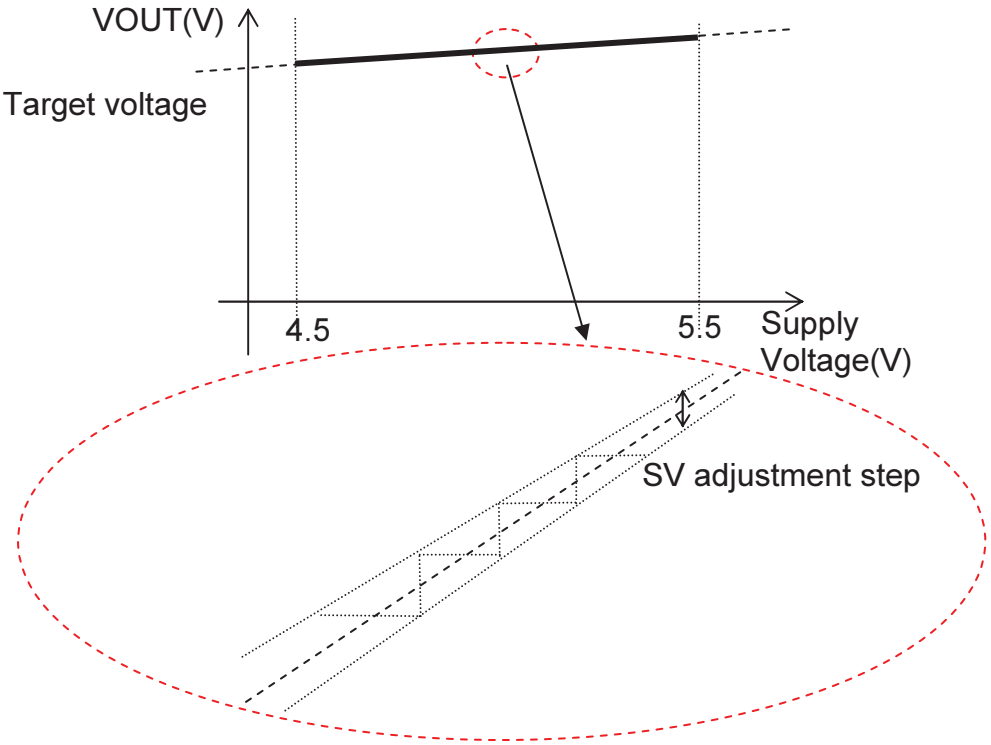
The hysteresis voltage to the detection threshold of the pressure detectors 1 and 2 is as follows by the detection threshold setup (Detect pressure above or below threshold).

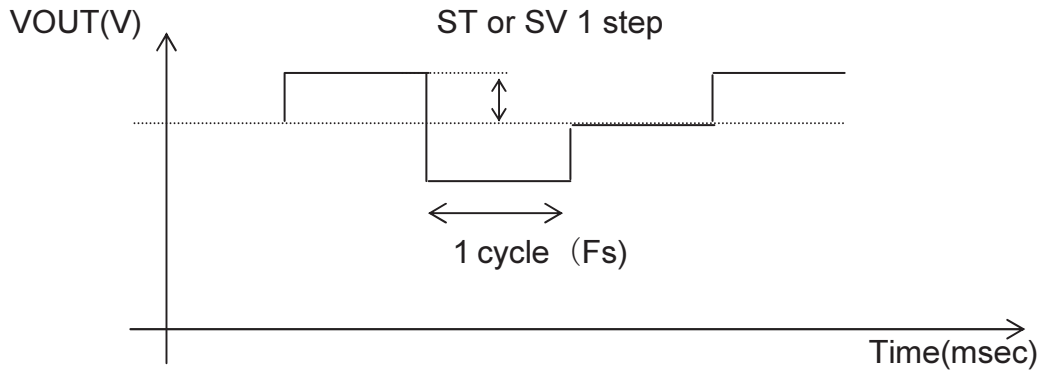
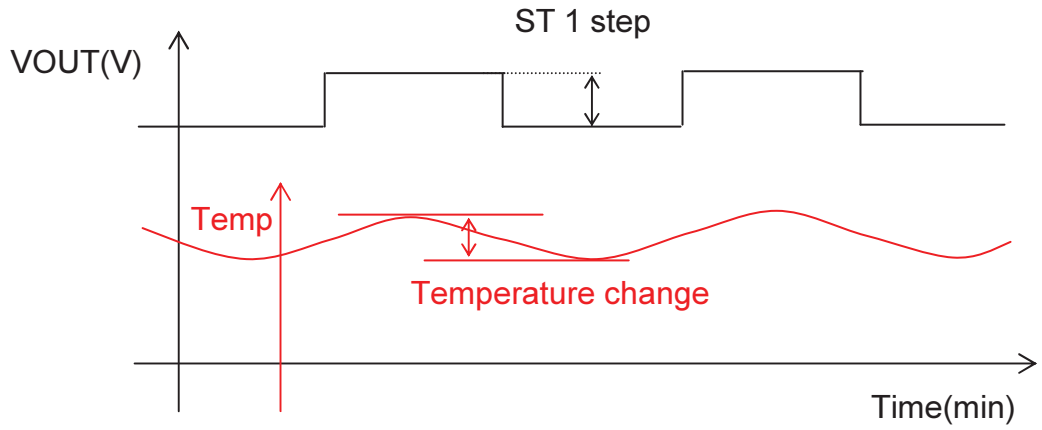
Detect pressure above threshold: Detection threshold – Hysteresis voltage
Detect pressure below threshold: Detection threshold + Hysteresis voltage

In addition, the setting range of “Detection threshold ± hysteresis voltage” should be set between from 0.125*VDD to 0.9*VDD (same setting range as the detection threshold of the pressure detector).

6) VOUT Output

The AK8998 VOUT output shows four kinds of output waveforms below according to the condition. Please use the AK8998 understanding of those output waveforms may come.

No	Item	Content
1	Description	**Sensitivity temperature variation characteristic (ST operation) :** When temperature changes, VOUT output shows sawtooth waveform within ST adjustment step, according to the pressure applied.
	Output Waveform	
2	Description	**Sensitivity supply voltage variation characteristic (SV operation) :** When supply voltage changes, VOUT output shows stepwise waveform within SV adjustment step , according to the pressure applied.
	Output Waveform	

No	Item	Content
3	Description	**VOUT output time change 1 :** When the band is not limited, a VOUT output shows stepwise change for every sampling period in the following figures. Since its change occurs for every sampling period, it can be reduced by using bandwidth shaping filter.
	Output Waveform	
4	Description	**VOUT output time change 2 :** When temperature changes slowly to compare with the band-limited time, a VOUT output shows stepwise change with temperature change in the following figures. For example, it occurs when the temperature in a thermostat chamber changes slowly.
	Output Waveform	

Serial Interface Description

The data of EEPROM and control register (volatile memory) in the AK8999 can be written and read through a two-wire serial interface, consisting of CSCLK pin and VOUT pin. When CSCLK=High is maintained beyond a definite period of time (1.0 msec), VOUT output will change from the Analog output to SDI/O (Serial data I/O).
And data is captured from VOUT synchronously with the rising edge of CSCLK after SDI/O shift. Input data contains three instruction bits (I2 - I0), five address bits (A4 - A0) and eight data bits (D7 - D0). Provide the data in the order of I2 → I0 → A4 → A0 → D7 → D0. And when CSCLK=Low is maintained beyond a definite period of time (0.5 msec), VOUT output will return from SDI/O to the Analog output.
On the WRITE instruction, allow 5msec or more write time for EEPROM and 10µsec or more write time for the control register (see Twr in 6) Digital AC Characteristics in the Electrical Characteristics section). For the READ instruction, data is written up to 8CLK for CSCLK and the data output starting at the rising edge of 9CLK is read out.

1) Data Configuration

Configuration of data written to or read out through the serial interface is shown below. There are 16 specific bits of data in total comprised of three instruction bits, five address bits and eight data bits.

Instruction			Address					Data							
I2	I1	I0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

←**Data input direction**

2) Description of Instructions

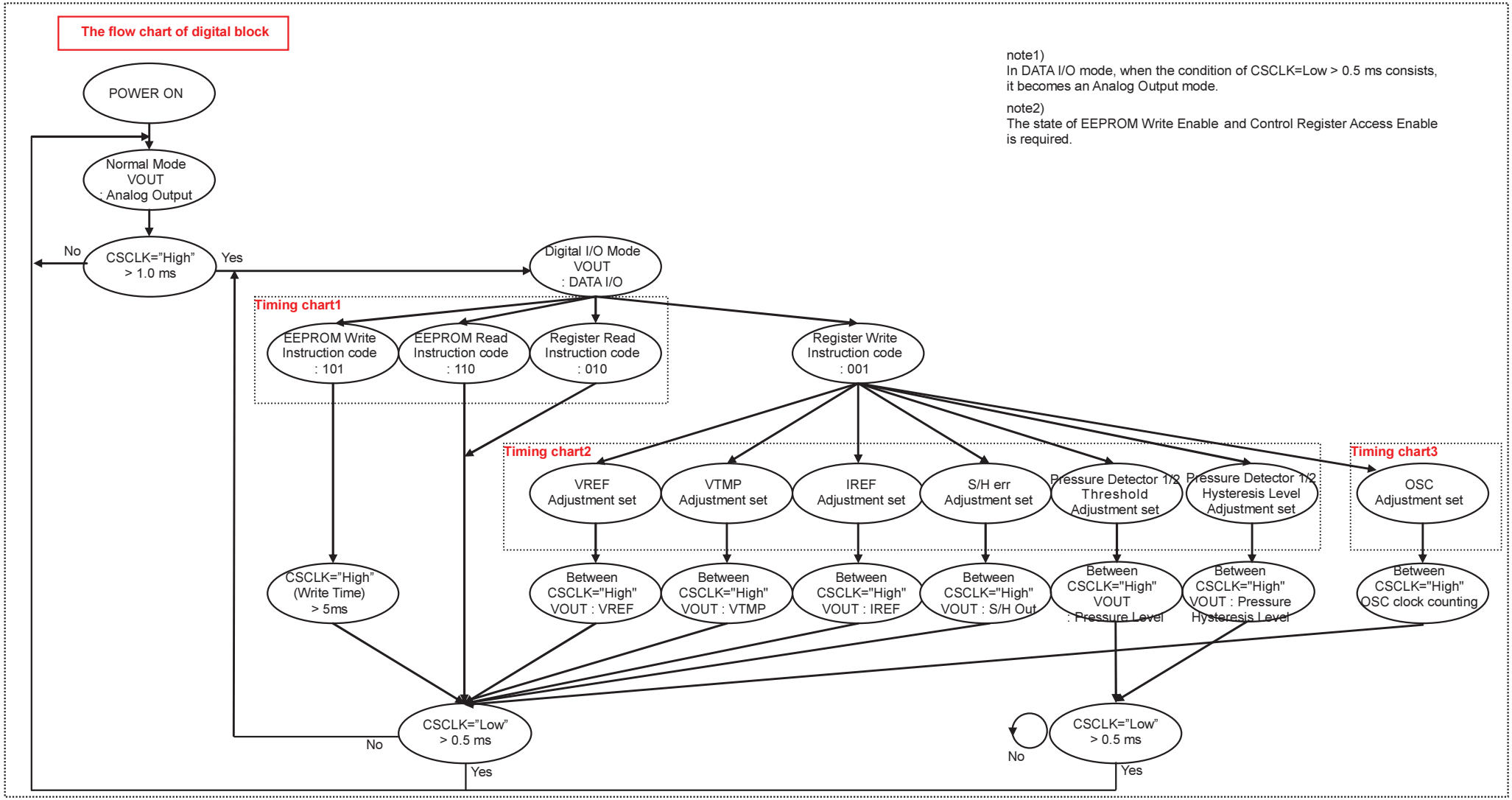
Instruction codes are summarized below.

Code Note 1)			Instruction	Description
I2	I1	I0		
1	1	0	EEPROM read (Read Mode)	Reads out the data written in the EEPROM
1	0	1	EEPROM write (Write Mode)	Writes data to the EEPROM. Write time (from 16th CSCLK rising edge to CSCLK falling edge) requires 5msec or more.
			EEPROM batch write (Write Mode)	If the 1Fh address is written, input data is written to all addresses except for 1Eh. Write time (from 16th CSCLK rising edge to CSCLK falling edge) requires 10msec or more.
0	1	0	Control reg. read (Read Mode)	Reads out the data written in the control register.
0	0	1	Control reg. write (Write Mode)	Writes the data to the control register. Write time (from 16th CSCLK rising edge to CSCLK falling edge) requires 10µsec or more.

Note) Instructions other than this are prohibited.

3) Flow chart of Digital block

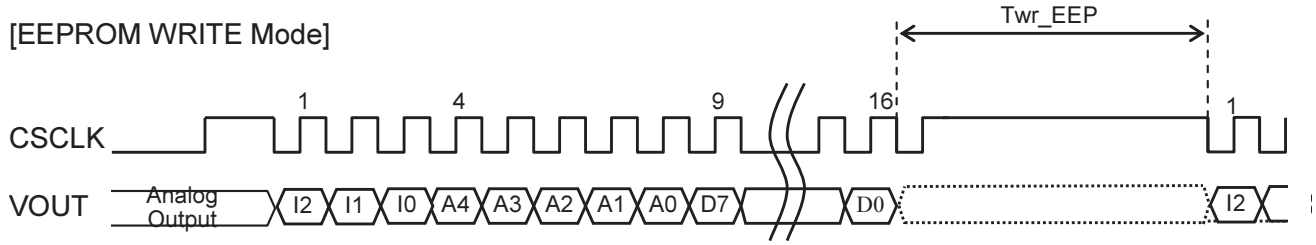
The flow chart of digital block is shown below.



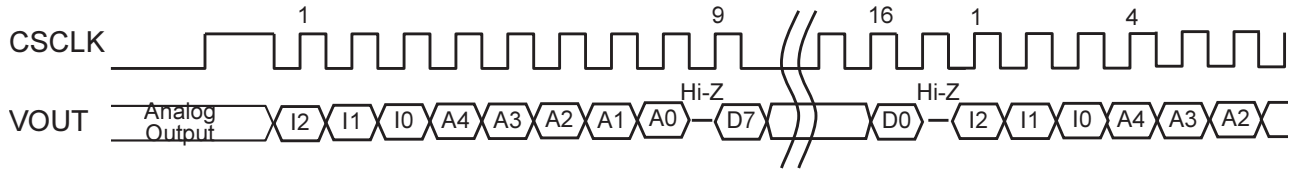
4) Serial Interface Timing Diagram

4.1) Timing chart 1

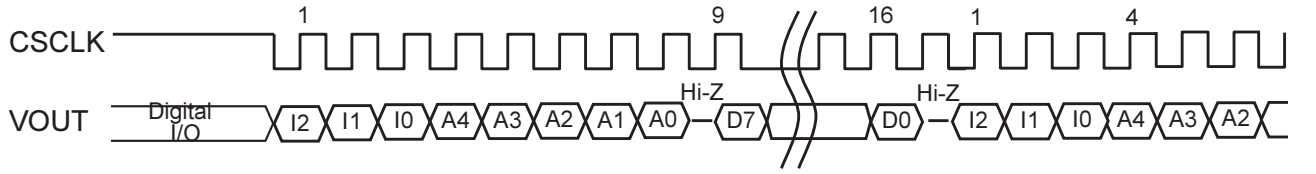
[EEPROM WRITE Mode]



[EEPROM READ Mode]

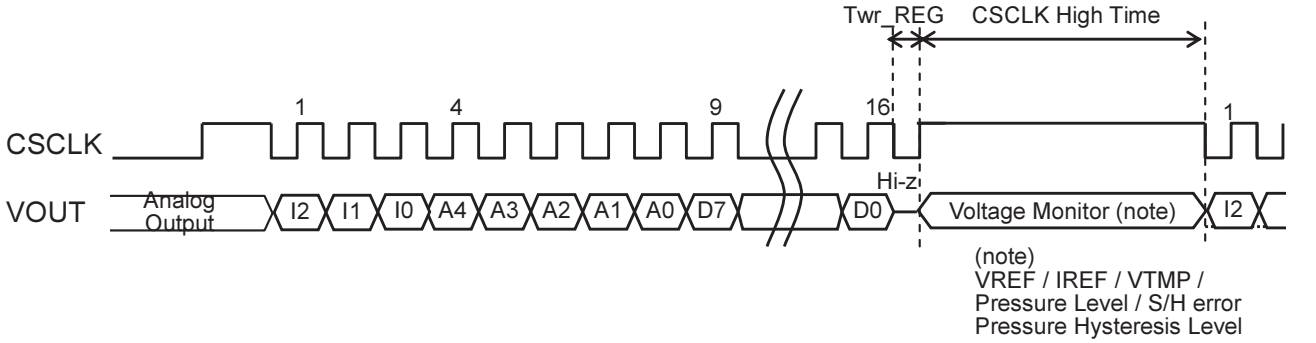


[Register READ Mode]



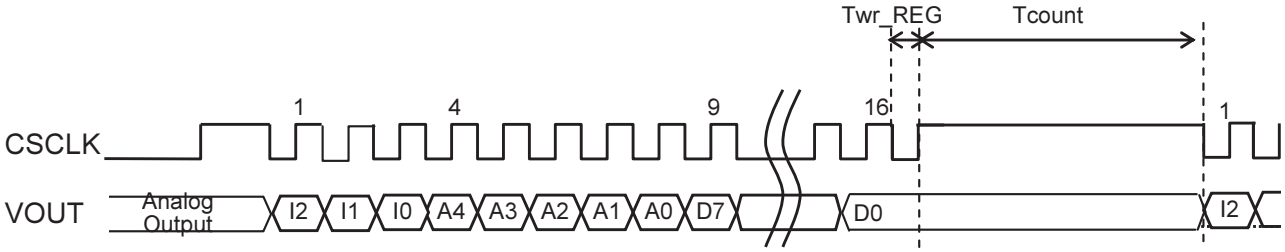
4.2) Timing chart 2

[Register Write Mode1]
VREF / IREF / VTMP / Pressure Level /Pressure Hysteresis Level / S/H error Adjustment set



4.3) Timing chart 3

[Register Write Mode2]
OSC Adjustment set



5) Register Map

5.1) EEPROM Map Plan

Name	Content	Address (hex)	Data Note 1) D7	D6	D5	D4	D3	D2	D1	D0
OCR	Offset voltage rough adj.	00h					EOCR[3]	EOCR[2]	EOCR[1]	EOCR[0]
							0	0	0	0
OCF	Offset voltage fine adj.	01h	EOCF[7]	EOCF[6]	EOCF[5]	EOCF[4]	EOCF[3]	EOCF[2]	ECCF[1]	EOCF[0]
			0	0	0	0	0	0	0	0
SC	Output span voltage adj.	02h	ESC[7]	ESC[6]	ESC[5]	ESC[4]	ESC[3]	ESC[2]	ESC[1]	ESC[0]
			0	0	0	0	0	0	0	0
OTS	Offset voltage temp. drift adj.	03h								EOT[8]
										0
OT	Offset voltage temp. drift adj.	04h	EOT[7]	EOT[6]	EOT[5]	EOT[4]	EOT[3]	EOT[2]	EOT[1]	EOT[0]
			0	0	0	0	0	0	0	0
STS	Sens. temp. drift adj.	05h								EST[8]
										0
ST	Sens. temp. drift adj.	06h	EST[7]	EST[6]	EST[5]	EST[4]	EST[3]	EST[2]	EST[1]	EST[0]
			0	0	0	0	0	0	0	0
PTH1	Pressure detector 1	07h	EINV1[0]	EINE1[0]	EIN1L[0]	EPT1[4]	EPT1[3]	EPT1[2]	EPT1[1]	EPT1[0]
			0	0	0	0	0	0	0	0
PTH2	Pressure detector 2	08h	EINV2[0]	EINE2[0]	EIN2L[0]	EPT2[4]	EPT2[3]	EPT2[2]	EPT2[1]	EPT2[0]
			0	0	0	0	0	0	0	0
HYS1 HYS2	Pressure detector comparator hysteresis voltage adj.	09h	EPTH1[0]				EHYS2[1]	EHYS2[0]	EHYS1[1]	EHYS1[0]
			0				0	0	0	0
LVS	Output ref. voltage adj.	0Ah								ELV[8]
										0
LV	Output ref. voltage adj.	0Bh	ELV[7]	ELV[6]	ELV[5]	ELV[4]	ELV[3]	ELV[2]	ELV[1]	ELV[0]
			0	0	0	0	0	0	0	0
ING	Input gain adj.	0Ch				EIG[4]	EIG[3]	EIG[2]	EIG[1]	EIG[0]
						0	0	0	0	0
MM1	Meas. mode	0Dh	EAGND[0]	EVPN[0]	ETMP[0]	ESCF[1]	ESCF[0]	EVD[1]	EVD[0]	ESF[0]
			0	0	0	0	0	0	0	0
VREF *	VREF voltage adj.	0Eh						EVR[2]	EVR[1]	EVR[0]
								0	0	0
IREF *	IREF current adj.	0Fh					EIR[3]	EIR[2]	EIR[1]	EIR[0]
							0	0	0	0
OSC *	OSC frequency adj.	10h					EFR[3]	EFR[2]	EFR[1]	EFR[0]
							0	0	0	0
VTMP *	VTMP adjustment	11h	ETM[7]	ETM[6]	ETM[5]	ETM[4]	ETM[3]	ETM[2]	ETM[1]	ETM[0]
			0	0	0	0	0	0	0	0
UE	User-writable data	12h	EUE[7]	EUE[6]	EUE[5]	EUE[4]	EUE[3]	EUE[2]	EUE[1]	EUE[0]
			0	0	0	0	0	0	0	0
STC	Sensitivity temperature drift adjustment range and VTMP adj.	13h							ETM[8]	ESTC[0]
									0	0
	Reserved	14h – 1Ch								
MM2	Control register access setup	1Dh								ETST[0]
										0
EWE	EEPROM Write Enable	1Eh								EWE[0]
										0
AW	EEPROM batch write mode	1Fh	EAW[7]	EAW[6]	EAW[5]	EAW [4]	EAW[3]	EAW[2]	EAW[1]	EAW[0]

Note 1) Lower line of each data represents the factory settings written to EEPROM.
Note 2) Access to the reserved addresses is prohibited.
Note 3) Write "0" to the unused D[7:0].
Note 4) For a packaged device, registers marked with * are adjusted before shipment. Therefore, defaults are not "0".

5.2) Control Register (Volatile Memory) Map

Name	Content	Address (hex)	Data Note 1) D7	D6	D5	D4	D3	D2	D1	D0
CM1	Adjustment mode	00h					**AM[3]**	**AM[2]**	**AM[1]**	**AM[0]**
							0	**0**	**0**	**0**
CM2	OSC variable ratio Note4)	01h	**CT[7]**	**CT[6]**	**CT[5]**	**CT[4]**	**CT[3]**	**CT[2]**	**CT[1]**	**CT[0]**
			0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SH1	S/H circuit output error adjustment 1	19h					SH1[3]		SH1[3]	
							0		0	
SH2	S/H circuit output error adjustment 2	10h			SH2[5]	SH2[4]		SH2[2]		
					0	0		0		
SH3	S/H circuit output error adjustment 3	12h		SH3[6]						
				0						
SH4	S/H circuit output error adjustment 4	17h					SH4[3]			
							0			
	Reserved	others								

Note 1) Lower line of each data represents the control register data upon power-up.
Note 2) Access to the reserved addresses is prohibited.
Note 3) Write "0" to the unused D[7:0].
Note 4) Access to this register serves as ReadOnly.

6) EEPROM and control register Description

6.1) Description of EEPROM

6.1.1) Adjustment Section EEPROM

Offset and span adjustment should be made after measurement mode setup and adjustment of the reference generator section including VREF, IREF, OSC and VTMP.

a) Offset voltage adjustment (EEPROM names: OCR, OCF)

Rough adjustment should be performed first, followed by a fine adjustment for the offset voltage. The content of the adjustment EEPROMs are shown here.

a-1) Offset voltage rough adjustment (OCR)

The offset voltage is adjusted roughly.
The offset adjustment voltage varies ratiometrically with respect to the supply voltage.
The ratio in the table below is benchmarked to a VOUT output of 4800 mV (@VDD: 5V) as 100% (ratio = (Offset voltage @VDD: 5V)/4800[mV]*100[%]).

Address : 00 hex D[3:0]=EOCR[3:0]

EOCR [2:0]			Ratio	VDD:3V		VDD:5V		Comments
Dec	Hex	Bin	(%)	EOCR [3]=0 (mV)	EOCR [3]=1 (mV)	EOCR [3]=0 (mV)	EOCR [3]=1 (mV)	
0	0	000	0.00	0	0	0	0	Default
1	1	001	33.33	800	-800	1600	-1600	
2	2	010	66.67	1600	-1600	3200	-3200	
3	3	011	100.00	2400	-2400	4800	-4800	
4	4	100	133.33	3200	-3200	6400	-6400	
5	5	101	166.67	4000	-4000	8000	-8000	
6	6	110	200.00	4800	-4800	9600	-9600	
7	7	111	233.33	5600	-5600	11200	-11200	

a-2) Offset voltage fine adjustment (OCF)

The offset voltage is adjusted finely.
The offset adjustment voltage varies ratiometrically with respect to the supply voltage.
The ratio in the table below is benchmarked to a VOUT output of 4800mV (@VDD: 5V) as 100% (ratio = (Offset voltage @VDD: 5V)/4800[mV]*100[%]).

Address : 01hex D[7:0]=EOCF[7:0]

EOCF [6:0]			Ratio	VDD:3V		VDD:5V		Comments
Dec	Hex	Bin	(%)	EOCF [7]=0 (mV)	EOCF [7]=1 (mV)	EOCF [7]=0 (mV)	EOCF [7]=1 (mV)	
0	00	0000000	0	0	0	0	0	Default
1	01	0000001	0.17	4	-4	8	-8	
:	:	:	:	:	:	:	:	
15	0F	0001111	2.50	60	-60	120	-120	
16	10	0010000	2.67	64	-64	128	-128	
:	:	:	:	:	:	:	:	
31	1F	0011111	5.17	124	-124	248	-248	
32	20	0100000	5.33	128	-128	256	-256	
:	:	:	:	:	:	:	:	
63	3F	0111111	10.50	252	-252	504	-504	
64	40	1000000	10.67	256	-256	512	-512	
:	:	:	:	:	:	:	:	
126	7E	1111110	21.00	504	-504	1008	-1008	
127	7F	1111111	21.17	508	-508	1016	-1016	

b) Output span voltage adjustment (EEPROM name: SC)

The span voltage is adjusted.
The magnification factor in this table represents an adjustment factor benchmarked to a VOUT output of 4800mV (@VDD: 5V) as 1 (factor) = 100[%]/100[%].
The output and sensitivity describes the adjustable output voltages with the assumed reference output (2400mV@VDD: 3V, 4800mV@VDD: 5V) when ESC[7:0] = 0 dec.

Address : 02 hex D[7:0]=ESC[7:0]

ESC[7:0]			Magnification	VDD:3V		VDD:5V		Comments
Dec	Hex	Bin	(Factor)	Output (mV)	Sens. (Factor)	Output (mV)	Sens. (Factor)	
0	00	00000000	100/100.00	2400	60.0	4800	60.0	Default
1	01	00000001	100/100.25	2394	59.9	4788	59.9	
2	02	00000010	100/100.50	2388	59.7	4776	59.7	
3	03	00000011	100/100.75	2382	59.6	4764	59.6	
4	04	00000100	100/101.00	2376	59.4	4752	59.4	
:	:	:	:	:	:	:	:	
123	7B	01111011	100/130.75	1836	45.9	3671	45.9	
124	7C	01111100	100/131.00	1832	45.8	3664	45.8	
125	7D	01111101	100/131.25	1829	45.7	3657	45.7	
126	7E	01111110	100/131.50	1825	45.6	3650	45.6	
127	7F	01111111	100/131.75	1822	45.5	3643	45.5	
128	80	10000000	100/132.00	1818	45.5	3636	45.5	Center
129	81	10000001	100/132.25	1815	45.4	3629	45.4	
130	82	10000010	100/132.50	1811	45.3	3623	45.3	
131	83	10000011	100/132.75	1808	45.2	3616	45.2	
132	84	10000100	100/133.00	1805	45.1	3609	45.1	
133	85	10000101	100/133.25	1801	45.0	3602	45.0	
:	:	:	:	:	:	:	:	
251	FB	11111011	100/162.75	1475	36.9	2949	36.9	
252	FC	11111100	100/163.00	1472	36.8	2945	36.8	
253	FD	11111101	100/163.25	1470	36.8	2940	36.8	
254	FE	11111110	100/163.50	1468	36.7	2936	36.7	
255	FF	11111111	100/163.75	1466	36.6	2931	36.6	

c) Offset voltage temperature drift adjustment (EEPROM name: OT)

The offset voltage temperature drift for the pressure sensor is adjusted, including the AK8998 internal error.
After performing the offset voltage adjustment at 25°C, use the EEPROM's offset voltage temperature characteristic coefficients for adjustment so that the absolute values of the AK8998's coefficient are matched to those of the sensor's coefficient.

Address : 03 hex - 04 hex D[8:0]=EOT[8:0]

EOT[7:0]			Ratio	VDD:3V		VDD:5V		Comments
Dec	Hex	Bin	(%)	EOT [8]=0 (mV/°C)	EOT [8]=1 (mV/°C)	EOT [8]=0 (mV/°C)	EOT [8]=1 (mV/°C)	
0	00	00000000	0.00	0.000	0.000	0.000	0.000	Default
1	01	00000001	0.39	0.087	-0.087	0.144	-0.144	
2	02	00000010	0.78	0.173	-0.173	0.289	-0.289	
3	03	00000011	1.18	0.260	-0.260	0.433	-0.433	
4	04	00000100	1.57	0.346	-0.346	0.577	-0.577	
:	:	:	:	:	:	:	:	
122	7A	01111010	47.84	10.564	-10.564	17.606	-17.606	
123	7B	01111011	48.24	10.650	-10.650	17.751	-17.751	
126	7E	01111110	49.41	10.910	-10.910	18.184	-18.184	
127	7F	01111111	49.80	10.997	-10.997	18.328	-18.328	
128	80	10000000	50.20	11.083	-11.083	18.472	-18.472	
129	81	10000001	50.59	11.170	-11.170	18.616	-18.616	
130	82	10000010	50.98	11.256	-11.256	18.761	-18.761	
131	83	10000011	51.37	11.343	-11.343	18.905	-18.905	
132	84	10000100	51.76	11.430	-11.430	19.049	-19.049	
133	85	10000101	52.16	11.516	-11.516	19.194	-19.194	
:	:	:	:	:	:	:	:	
236	EC	11101100	92.55	20.435	-20.435	34.058	-34.058	
237	ED	11101101	92.94	20.521	-20.521	34.202	-34.202	
238	EE	11101110	93.33	20.608	-20.608	34.347	-34.347	
239	EF	11101111	93.73	20.695	-20.695	34.491	-34.491	
:	:	:	:	:	:	:	:	
255	FF	11111111	100.00	22.080	-22.080	36.800	-36.800	

d) Sensitivity temperature drift adjustment range change (EEPROM name: ESTC)

The adjustment range of the sensitivity temperature drift coefficient is changed.
By setting the sensitivity temperature drift coefficient adjustment range (ESTC [0]) as "H", the sensitivity temperature drift coefficient adjustment range will be set from +2500 ppm/°C to -4000ppm/°C. By setting "L" is used, it will be set from +1000 ppm/°C to -2500 ppm/°C.

Address : 13 hex D[0]= ESTC[0]

D[0]	Symbol	Mode setup
D[0]	ESTC[0]	Sensitivity temperature drift adjustment range change
0	ST25	Sensitivity temperature drift adjustment range : -2500ppm/°C to +1000ppm/°C (Default)
1	ST40	Sensitivity temperature drift adjustment range : -4000ppm/°C to +2500ppm/°C

e) Sensitivity temperature drift adjustment (EEPROM name: ST)

The sensitivity temperature drift for the pressure sensor is adjusted, including the AK8998 internal error.
After performing the span voltage adjustment at 25ºC, use the EEPROM's sensitivity temperature drift coefficients for adjustment so that the absolute values of the AK8998's coefficient are matched to those of the sensor's coefficient.

Address : 05 hex - 06 hex D[8:0]=EST[8:0]

EST[7:0]			Ratio	VDD:3V		VDD:5V		Comments
Dec	Hex	Bin	(%)	EST [8]=0 (ppm/°C)	EST [8]=1 (ppm/°C)	EST [8]=0 (ppm/°C)	EST [8]=1 (ppm/°C)	
0	0	00000000	0.00	0	0	0	0	Default
1	1	00000001	0.39	18	-18	18	-18	
2	2	00000010	0.78	36	-36	36	-36	
:	:	:	:	:	:	:	:	
25	19	00011001	9.80	451	-451	451	-451	
26	1A	00011010	10.20	469	-469	469	-469	
27	1B	00011011	10.59	487	-487	487	-487	
28	1C	00011100	10.98	505	-505	505	-505	
:	:	:	:	:	:	:	:	
137	89	10001001	53.73	2471	-2471	2471	-2471	
138	8A	10001010	54.12	2489	-2489	2489	-2489	
139	8B	10001011	54.51	2507	-2507	2507	-2507	
140	8C	10001100	54.90	2525	-2525	2525	-2525	
:	:	:	:	:	:	:	:	
220	DC	11011100	86.27	3969	-3969	3969	-3969	
221	DD	11011101	86.67	3987	-3987	3987	-3987	
222	DE	11011110	87.06	4005	-4005	4005	-4005	
223	DF	11011111	87.45	4023	-4023	4023	-4023	
:	:	:	:	:	:	:	:	
254	FE	11111110	99.61	4582	-4582	4582	-4582	
255	FF	11111111	100.00	4600	-4600	4600	-4600	

Note) When ESTC[0] is set to 1hex, adjust in -4000ppm/°C to +2500 ppm/°C. When ESTC[0] is set to 0hex, adjust in -2500ppm/°C to +1000 ppm/°C.

f) Pressure detector 1 (EEPROM name: PTH1, HYS1)

The operating mode, the detection threshold values and the hysteresis voltage of the comparator for the pressure detector 1 are individually set up.
The detector threshold voltage varies and the hysteresis voltage ratiometrically with respect to the supply voltage.

f-1) Pressure detector operating mode setup

Address : 07 hex D[7:5] = EINV1[0], EINE1[0], EIN1L[0]

D[7:5]	Symbol	Mode setup
D[7]	EINV1[0]	Pressure detector output polarity setup EEPROM
0	EINV11	High output when detected (default)
1	EINV10	Low output when detected
D[6]	EINE1[0]	Pressure detector enabled setup EEPROM
0	INT1E	Pressure detector 1 enable (default)
1	INT1D	Pressure detector 1 disable
D[5]	EIN1L[0]	Pressure detector 1 detection threshold setup EEPROM
0	INT1<	Detect pressure above threshold (default)
1	INT1>	Detect pressure below threshold

Address : 09 hex D[7] = EPTH1[0]

D[7]	Symbol	Mode setup
D[7]	EPTH1[0]	Pressure detector 1 detection threshold selection EEPROM
0	PTH1R	EEPROM setup (default)
1	PTH1E	DET2/PTH pin external setup

f-2) Pressure detector detection threshold adjustment

Address : 07 hex D[4:0]=EPT1[4:0]

EPT1[4:0]			Detection threshold (V)		Comments
Dec	Hex	Bin	Detect threshold	ex. VDD:5V	
-16	10	10000	0.900*VDD	4.500	
-15	11	10001	0.875*VDD	4.375	
-14	12	10010	0.850*VDD	4.250	
:	:	:	:	:	
-3	1D	11101	0.575*VDD	2.875	
-2	1E	11110	0.550*VDD	2.750	
-1	1F	11111	0.525*VDD	2.625	
0	00	00000	0.500*VDD	2.500	Default
1	01	00001	0.475*VDD	2.375	
2	02	00010	0.450*VDD	2.250	
:	:	:	:	:	
14	0E	01110	0.150*VDD	0.750	
15	0F	01111	0.125*VDD	0.625	

f-3) Comparator hysteresis voltage adjustment for pressure detection

Address : 09 hex D[1:0]=EHYS1[1:0]

EHYS1[1:0]			Hysteresis voltage (mV)		Comments
Dec	Hex	Bin	Hysteresis voltage	ex. VDD:5V	
2	2	10	0.030*VDD	150.0	
3	3	11	0.040*VDD	200.0	
0	0	00	0.050*VDD	250.0	Default
1	1	01	0.060*VDD	300.0	

g) Pressure detector 2 (EEPROM name: PTH2, HYS2)

The operating mode, the detection threshold values and the hysteresis voltage of the comparator for the pressure detector 2 are individually set up.
The detector threshold voltage varies and the hysteresis voltage ratiometrically with respect to the supply voltage.

g-1) Pressure detector operating mode setup

Address : 08 hex D[7:5] = EINV2[0], EINE2[0], EIN2L[0]

D[7:5]	Symbol	Mode setup
D[7]	EINV2[0]	Pressure detector output polarity setup EEPROM
0	EINV21	High output when detected (default)
1	EINV20	Low output when detected
D[6]	EINE2[0]	Pressure detector enabled setup EEPROM
0	INT2E	Pressure detector 2 enable (default)
1	INT2D	Pressure detector 2 disable
D[5]	EIN2L[0]	Pressure detector 2 detection threshold setup EEPROM
0	INT2<	Detect pressure above threshold (default)
1	INT2>	Detect pressure below threshold

g-2) Pressure detector detection threshold adjustment

Address : 08 hex D[4:0]=EPT2[4:0]

EPT2[4:0]			Detection threshold (V)		Comments
Dec	Hex	Bin	Detect threshold	ex. VDD:5V	
-16	10	10000	0.900*VDD	4.500	
-15	11	10001	0.875*VDD	4.375	
-14	12	10010	0.850*VDD	4.250	
:	:	:	:	:	
-3	1D	11101	0.575*VDD	2.875	
-2	1E	11110	0.550*VDD	2.750	
-1	1F	11111	0.525*VDD	2.625	
0	00	00000	0.500*VDD	2.500	Default
1	01	00001	0.475*VDD	2.375	
2	02	00010	0.450*VDD	2.250	
:	:	:	:	:	
13	0D	01101	0.175*VDD	0.875	
14	0E	01110	0.150*VDD	0.750	
15	0F	01111	0.125*VDD	0.625	

g-3) Comparator hysteresis voltage adjustment for pressure detection

Address : 09 hex D[3:2]=EHYS2[1:0]

EHYS2[1:0]			Hysteresis voltage (mV)		Comments
Dec	Hex	Bin	Hysteresis voltage	ex. VDD:5V	
2	2	10	0.030*VDD	150.0	
3	3	11	0.040*VDD	200.0	
0	0	00	0.050*VDD	250.0	Default
1	1	01	0.060*VDD	300.0	

h) Output reference voltage adjustment (EEPROM names: LVS, LV)

Adjusts the output reference voltage.
The content of the adjustment EEPROMs is shown here.

Address : 0A hex - 0B hex D[8:0]=ELV[8:0]

ELV[7:0]			VOUT pin (x VDD)		Comments
Dec	Hex	Bin	ELV[8]=0h	ELV[8]=1h	
0	00	00000000	0.500	0.500	Default
1	01	00000001	0.498	0.502	
2	02	00000010	0.496	0.504	
3	03	00000011	0.494	0.506	
4	04	00000100	0.492	0.508	
:	:	:	:	:	
124	7C	01111100	0.252	0.748	
125	7D	01111101	0.250	0.750	
126	7E	01111110	0.248	0.752	
127	7F	01111111	0.246	0.754	
128	80	10000000	0.244	0.756	
:	:	:	:	:	
240	F0	11110000	0.020	0.980	
241	F1	11110001	0.018	0.982	
242	F2	11110010	0.016	0.984	
243	F3	11110011	0.014	0.986	
:	:	:	:	:	
250	FA	11111010	0.000	1.000	
251	FB	11111011	0.000	1.000	
252	FC	11111100	0.000	1.000	
253	FD	11111101	0.000	1.000	
254	FE	11111110	0.000	1.000	
255	FF	11111111	0.000	1.000	

i) Input gain adjustment (EEPROM name: ING)

EEPROM for setting the total gain.
The input gain is adjusted according to the full-scale voltage of the pressure sensor.

i-1) Sensitivity temperature drift adj. range: -4000ppm/°C to +2500ppm/°C (ESTC[0]=1h)

Address : 0C hex D[4:0]=EIG[4:0]

EIG[3:0]			G1 Gain (times)	Total Gain (times)		Comments
Dec	Hex	Bin		EIG[4]=0 G2: 3x	EIG[4]=1 G2: 1.5x	
0	0	0000	70.0	210.0	105.0	Default
1	1	0001	60.0	180.0	90.0	
2	2	0010	50.0	150.0	75.0	
3	3	0011	40.0	120.0	60.0	
4	4	0100	35.0	105.0	52.5	
5	5	0101	30.0	90.0	45.0	
6	6	0110	25.0	75.0	37.5	
7	7	0111	20.0	60.0	30.0	
8	8	1000	15.0	45.0	22.5	
9	9	1001	12.0	36.0	18.0	
10	A	1010	10.0	30.0	15.0	
11	B	1011	7.0	21.0	10.5	
12	C	1100	5.0	15.0	7.5	
13	D	1101	Setup prohibited	Setup prohibited	Setup prohibited	
14	E	1110				
15	F	1111				

i-2) Sensitivity temperature drift adj. range: -2500ppm/°C to +1000ppm/°C (ESTC[0]=0h)

Address : 0C hex D[4:0]=EIG[4:0]

EIG[3:0]			G1 Gain (times)	Total Gain (times)		Comments
Dec	Hex	Bin		EIG[4]=0 G2: 2.352x	EIG[4]=1 G2: 1.176x	
0	0	0000	70.0	164.7	82.4	初期値
1	1	0001	60.0	141.2	70.6	
2	2	0010	50.0	117.6	58.8	
3	3	0011	40.0	94.1	47.1	
4	4	0100	35.0	82.4	41.2	
5	5	0101	30.0	70.6	35.3	
6	6	0110	25.0	58.8	29.4	
7	7	0111	20.0	47.1	23.5	
8	8	1000	15.0	35.3	17.6	
9	9	1001	12.0	28.2	14.1	
10	A	1010	10.0	23.5	11.8	
11	B	1011	7.0	16.5	8.2	
12	C	1100	5.0	11.8	5.9	
13	D	1101	Setup prohibited	Setup prohibited	Setup prohibited	
14	E	1110				
15	F	1111				

j) measurement mode setup (EEPROM name: MM)

EEPROM is used for setting up the measurement mode for the AK8998.
A setup of a sampling frequency, supply voltage & sensor drive voltage, the enable / disable of Internal SCF & SMF, the internal / external of a temperature sensor, and the internal switching of VP & VN can be performed.

Address : 0D hex D[7:0]= EAGND[0], EVPN[0], ETMP[0], ESCF[1:0], EVD[1:0], ESF[0]

D[7:0]	Symbol	Mode setup
D[7]	EAGND[0]	AGND pin setup EEPROM
0	AGNDD	AGND pin disable (default)
1	AGNDE	AGND pin enable
D[6]	EVPN[0]	VP & VN internal switching EEPROM
0	VPNN	VP->VP, VN->VN (default)
1	VPNR	VP->VN, VN->VP
D[5]	ETMP[0]	Temperature sensor Internal & External change EEPROM
0	TMPE	External temperature sensor use (default) *Cannot be used in Sampling frequency as 1kHz (ESF[0]=1h).
1	TMPI	Internal temperature sensor use
D[4:3]	ESCF[1:0]	Internal SCF & SMF setup EEPROM
00	SCDS	Internal SCF & SMF disable (default)
01	SCEN1	Internal SCF & SMF enable & Cutoff frequency 1kHz
10	SCEN2	Internal SCF & SMF enable & Cutoff frequency 500Hz
11	SCEN3	Internal SCF & SMF enable & Cutoff frequency 250Hz
D[2:1]	EVD[1:0]	Supply voltage & sensor drive voltage setup EEPROM
00	VDD504	Supply voltage at 5V & sensor drive voltage at 4V (default)
01	VDD502	Supply voltage at 5V & sensor drive voltage at 2.2V
10	VDD332	Supply voltage at 3.3V & sensor drive voltage at 2.2V
11	VDD302	Supply voltage at 3V & sensor drive voltage at 2.2V
D[0]	ESF[0]	Sampling frequency setup EEPROM
0	SF10	Sampling frequency 10kHz (default)
1	SF1	Sampling frequency 1kHz *Cannot be used at the time of External temperature sensor is used (ETMP[0]=0h).

6.1.2) Reference Voltage Generator EEPROM

k) VREF voltage adjustment (EEPROM name: VREF)

EEPROM for adjusting the AK8998 reference voltage. Perform an adjustment to attain the reference voltage of 1000 mV (See Recommended Connection Examples for Components).
ΔVREF3/5 in the table below indicates a value varying with the setup values of the EEPROM.
ΔVS3/5 represents the values of ΔVREF3/5 multiplied by two and four, respectively. The ratio is benchmarked to 1000mV (VREF ideal value) as 100% (Ratio = (ΔVREF3/5) /1000[mV]*100[%]).

Address : 0E hex D[2:0]=EVR[2:0]

EVR[2:0]			Ratio	VDD: 3V, 3.3V mode		VDD:5V		Comments
Dec	Hex	Bin	(%)	ΔVREF3 (mV)	ΔVS3 (mV)	ΔVREF5 (mV)	ΔVS5 (mV)	
-4	4	100	-4	-40	-80	-40	-160	
-3	5	101	-3	-30	-60	-30	-120	
-2	6	110	-2	-20	-40	-20	-80	
-1	7	111	-1	-10	-20	-10	-40	
0	0	000	0	0	0	0	0	Default
1	1	001	1	+10	+20	+10	+40	
2	2	010	2	+20	+40	+20	+80	
3	3	011	3	+30	+60	+30	+120	

l) IREF current adjustment (EEPROM name: IREF)

EEPROM for adjusting the AK8998 reference current. The external resistor (1MΩ) is connected to VOUT pin. Reference current is supplied to external resistor, and it adjusts so that the voltage across the both ends of external resistor may be set to 1.0V (See Recommended Connection Examples for Components).
IREF in the table below indicates a current value with the setup values of the EEPROM.
VIREF (=IREF*1[MΩ]) is a voltage value varying with the external resistance (1MΩ) at the time of adjustment. The ratio is benchmarked to 1.0μA (IREF ideal value) as 100% (Ratio = (IREF-1.0 [μA])/1.0 [μA]*100[%]).

Address : 0F hex D[3:0]=EIR[3:0]

EIR[3:0]			Ratio	IREF	VIREF	Comments
Dec	Hex	Bin	(%)	(μA)	(V)	
-8	8	1000	-17.0	0.830	0.830	
-7	9	1001	-15.2	0.848	0.848	
-6	A	1010	-13.4	0.866	0.866	
-5	B	1011	-11.5	0.885	0.885	
-4	C	1100	-9.5	0.905	0.905	
-3	D	1101	-7.3	0.927	0.927	
-2	E	1110	-5.0	0.950	0.950	
-1	F	1111	-2.6	0.974	0.974	
0	0	0000	0.0	1.000	1.000	Default
1	1	0001	2.8	1.028	1.028	
2	2	0010	5.7	1.057	1.057	
3	3	0011	8.8	1.088	1.088	
4	4	0100	12.2	1.122	1.122	
5	5	0101	15.9	1.159	1.159	
6	6	0110	19.8	1.198	1.198	
7	7	0111	24.1	1.241	1.241	

m) OSC frequency adjustment (EEPROM name: OSC)

EEPROM for adjusting the AK8998 operation clock. Perform an adjustment to attain a frequency of 1000kHz. Reading the ratio data from the OSC variable ratio register (CT[7:0]), the adjustment data of the OSC frequency adjustment EERPOM is calculated.
Frequency Δf in the table below indicates a value varying with the setup values of the EEPROM. The ratio is benchmarked to 1.000kHz (OSC ideal value) as 100% (Ratio = Frequency Δf/(Frequency Δf+1000[kHz])*100[%]).

Address : 10 hex D[3:0]=EFR[3:0]

EFR[3:0]			Ratio	Frequency Δf	Comments
Dec	Hex	Bin	(%)	(kHz)	
-5	B	1011	-34	-251	
-4	C	1100	-25	-197	
-3	D	1101	-17	-146	
-2	E	1110	-11	-99	
-1	F	1111	-5	-52	
0	0	0000	0	0	Default
1	1	0001	5	49	
2	2	0010	10	106	
3	3	0011	14	162	
4	4	0100	18	224	
5	5	0101	22	274	
6	6	0110	25	329	
7	7	0111	28	384	

Note1) Hex 8 to A are prohibited for setup.

n) VTMP voltage adjustment (EEPROM name: VTMP)

Compensates the offset values for the AK8998's internal temperature sensor and external temperature sensor. Adjusts the values so that the difference between VTMP voltage and VREF voltage is close to 0 mV (If VREF is 1005mV, adjust so that VTMP is also 1005mV).
The rough adjustment (ETM[8:6]) is invalid when the internal temperature sensor is used (ETMP[0]="H"). The rough adjustment is effective when the external temperature sensor is used (ETMP[0]="L").
ΔVTMP in the table below indicates a value varying with the setup values of the EEPROM. The ratio is benchmarked to 1000mV (VREF ideal value) as 100% (Ratio = ΔVTMP/1000[mV]*100[%]).

Address : 11 hex D[5:0]=ETM[5:0]

ETM[5:0]			Ratio	ΔVTMP	Comments
Dec	Hex	Bin	(%)	(mV)	
-32	20	100000	+6.4	+64	
.....					
-16	30	110000	+3.2	+32	
.....					
-8	38	111000	+1.6	+16	
.....					
-4	3C	111100	+0.8	+8	
.....					
-1	3F	111111	+0.2	+2	
0	00	000000	0.0	0	Default
1	01	000001	-0.2	-2	
.....					
4	04	000100	-0.8	-8	
.....					
8	08	001000	-1.6	-16	
.....					
16	10	010000	-3.2	-32	
.....					
31	1F	011111	-6.2	-62	

Address : 11 hex D[7:6]=ETM[7:6], 13 hex D[1]=ETM[8]

ETM[8:6]			Ratio	ΔVTMP	Comments
Dec	Hex	Bin	(%)	(mV)	
4	4	100	Setup prohibited	Setup prohibited	
5	5	101	Setup prohibited	Setup prohibited	
6	6	110	+17.0	+170	
7	7	111	+8.5	+85	
0	0	000	0.0	0	Default
1	1	001	-8.5	-85	
2	2	010	-17.0	-170	
3	3	011	Setup prohibited	Setup prohibited	

o) User-writable data space (EEPROM name: UE)

Free area (EEPROM) available to the user.

Address : 12 hex D[7:0]=EUE[7:0]

Name	Content	Address	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
UE	User-writable data	12 hex	EUE7	EUE6	EUE5	EUE4	EUE3	EUE2	EUE1	EUE0
Default			0	0	0	0	0	0	0	0

p) Control register access setup (EEPROM name: MM2)

The access setup to the control register (volatile memory) is performed.
When the control register access setup is disabled (ETST[0]=0h), the control register (C address: 00h) is fixed to the initial value, and cannot be accessed, unless control register access is validated.

Address : 1D hex D[0]= ETST[0]

D[0]	Symbol	Mode setup
D[0]	ETST[0]	Control register access setup
0	TSTDS	Control register access disable(default)
1	TSTEN	Control register access enable

q) EEPROM Write Enable setup (EEPROM name:EWE)

The EEPROM write enable setup is performed.
When the setup of EEPROM Write Enable is validated (EWE[0]=1h), the writing to EEPROM is permitted. If it is invalid, the writing to EEPROM other then EEPROM Write Enable (address: 00 -1Dh, 1Fh) becomes impossible. And this address cannot be written by batch writing. However, EEPROM read (all the addresses) is possible even in that case.

Address : 1E hex D[0]= EWE[0]

D[0]	Symbol	Mode setup
D[0]	EWE[0]	EEPROM Write Enable setup
0	WEDS	EEPROM Write disable (default)
1	WEEN	EEPROM Write enable

r) EEPROM batch write mode (EEPROM name: AW)

Initializes the addresses 00 hex to 1D hex in the EEPROM map at once or writes identical data. This address is not available in the EEPROM.

Address : 1F hex D[7:0]=EAW[7:0]

Name	Content	Address	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
AW	EEPROM batch write	1F hex	EAW7	EAW6	EAW5	EAW4	EAW3	EAW2	EAW1	EAW0

6.2) Description of Control Register (Volatile Memory)

a) Adjustment mode (Register name: CM1)

This register is used to adjust the AK8998 reference voltage and pressure sensor's offset, span, offset temperature drift and sensitivity temperature drift including those of the AK8998. In addition, the value of the register returns to the initial value on the following conditions.

- At the power up
- When CSCLK=Low is maintained 0.5msec or more
- When ETST[0] is set to "L"

Address : 00 hex D[3:0]=AM[3:0]
(This is not a nonvolatile EEPROM, but a volatile register.)

D[7:0]	Symbol	Mode setup	Description
D[7:4]			Reserved
D[3:0]	AM[3:0]	IC adjustment mode	
0000			(default)
0001	AVR	VREF adjustment	The VREF voltage is output at the VOUT pin.
0010	AIR	IREF adjustment	The IREF current is output at the VOUT pin.
0011	AFR	OSC adjustment	Input the fixed period of High level (2.0msec) from the CSCLK pin. The count value in the internal counter is stored in the register.
0100	ATO	VTMP adjustment	The VTMP voltage is output at the VOUT pin. Adjust this voltage so that it matches the VREF voltage at 25°C.
0101	ADT1	judge threshold 1 adjustment	The internally set judge threshold value 1 is output at the VOUT pin.
0110	ADT2	judge threshold 2 adjustment	The internally set judge threshold value 2 is output at the VOUT pin.
0111	AHY1	hysteresis voltage 1	The hysteresis voltage of the comparator 1 is output at the VOUT pin.
1000	AHY2	hysteresis voltage 2	The hysteresis voltage of the comparator 2 is output at the VOUT pin.
1001-1111		Reserved	

b) OSC variable ratio storing register (Register name: CM2)

It is used for adjustment of the oscillator frequency of AK8998. The counted value in the internal counter is stored. Since the internal counter is overflowing when a count value shows FF hex, measure again by re-defining High level period.
This register is readonly. In addition, the value of the register returns to the initial value on the following conditions.

- At the power up
- When CM1 register is written
- When CSCLK=Low is maintained 0.5msec or more
- When ETST[0] is set to "L"

Address : 01 hex D[7:0]=CT[7:0]
(This is not a nonvolatile EEPROM, but a volatile register.)

CT[7:0]			Count value	Ratio	Comments
Dec	Hex	Bin	(time)	(%)	
0	00	00000000	0	0	Default
1	01	00000001	1	-99	
:	:	:	:	:	
98	62	01100010	98	-2	
99	63	01100011	99	-1	
100	64	01100100	100	0	Ideal value
101	65	01100101	101	1	
102	66	01100110	102	2	
:	:	:	:	:	
254	FE	11111110	254	154	
255	FF	11111111	-	-	Counter error

c) S/H circuit output error adjustment register (Register name: SH1 to SH4)

It is used for adjustment of the S/H circuit output error of AK8998.
The value of the register returns to the initial value on the following conditions.

- At the power up
- When CSCLK=Low is maintained 0.5msec or more

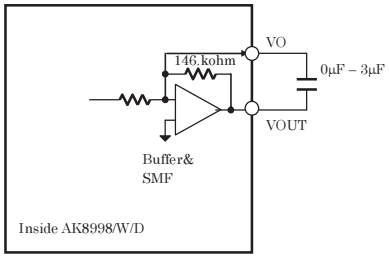
It is necessary to set up a register in order of the following.
(This is not a nonvolatile EEPROM, but a volatile register.)

No.	Register Name	Address	Data	Comments
1	SH1	19hex	0Ahex	
2	SH2	10hex	34hex	
3	SH3	12hex	40hex	
4	SH4	17hex	08hex	

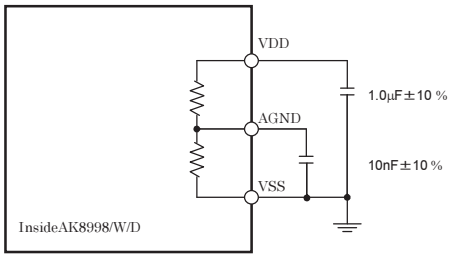
Note) Other Data is prohibited for setup.

Recommended Connection Examples for Components

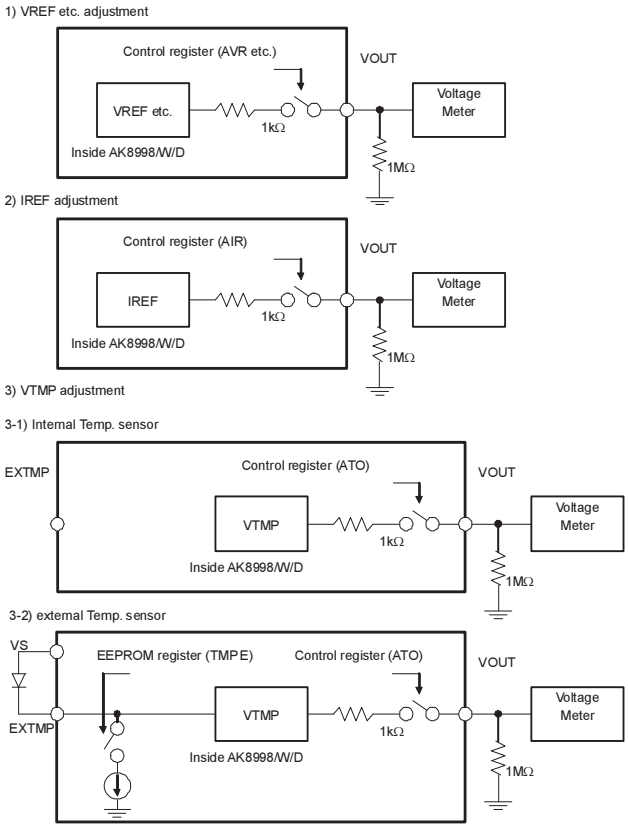
1) VO pin connection example



2) Power supply pin connection example

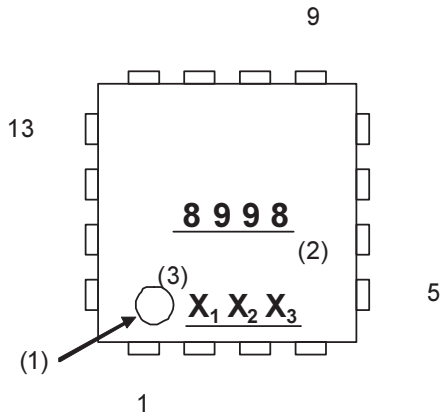


3) VOUT pin connection examples for adjustment



Package Information

1. Marking



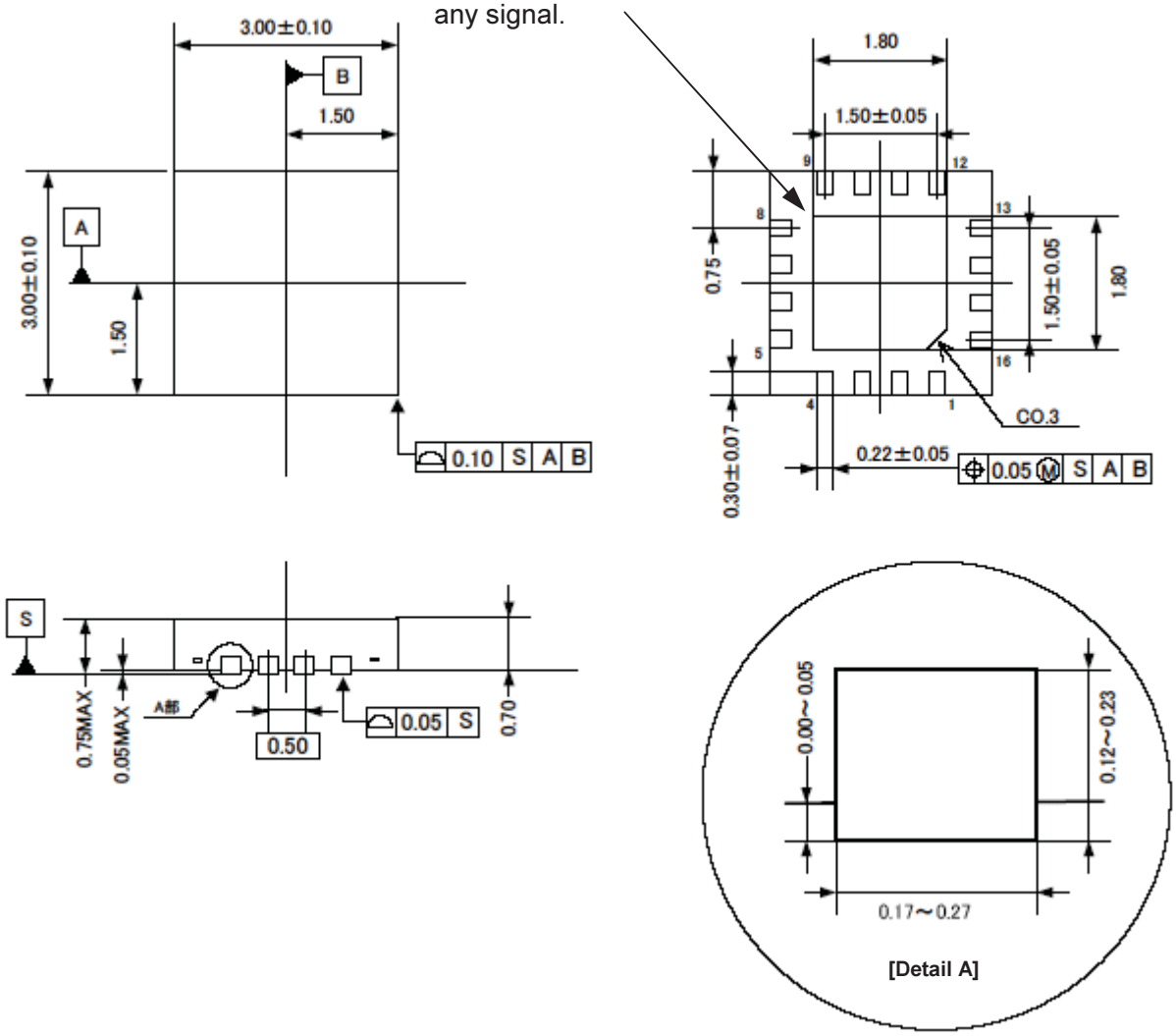
(1) Pin Number 1 indication mark

(2) Part Number

(3) Date Code (3 digits)

2. External Dimensions

The rear-side TAB is recommended to be mounted on the substrate to ensure strength. Do not connect to the power supply, GND or any signal.



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