DATA SHEET

74F543

Octal registered transceiver, non-inverting (3-State)

Product data sheet
Replaces data sheet 74F543/74F544 of 1994 Dec 05

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Philips
Semiconductors

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Octal registered transceiver, non-inverting (3-State) 74F543

FEATURES

- Combines74F245 and 74F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 20 mA and source 3 mA
- B outputs sink 64 mA and source 15 mA
- 3-State outputs for bus-oriented applications
- Available in SSOP Type II package

DESCRIPTION

The 74F543 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA, while the B outputs are rated for 64 mA.

FUNCTIONAL DESCRIPTION

The 74F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be LOW in order to enter data from A0 - A7 or take data from B0 - B7, as indicated in the Function Table. With $\overline{EAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition for the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0 ns	80 mA

ORDERING INFORMATION

Commerical range: V_{CC} = 5 V ± 10 %; T_{amb} = 0 °C to +70 °C

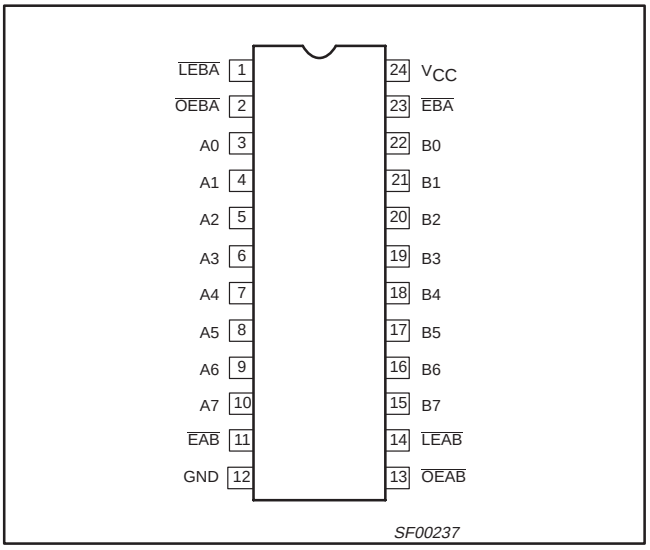
Type number	Package		
	Name	Description	Version
N74F543D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F543DB	SSOP24	plastic shrink small outline pacakge; 24 leads; body width 5.3 mm	SOT340-1
N74F543N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222–1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

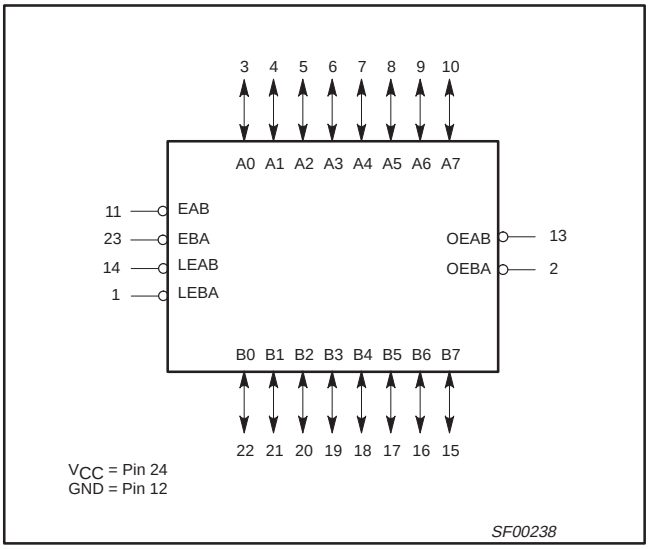
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7	Port A, 3-State inputs	3.5/1.0	70 µA/0.6 mA
B0 - B7	Port B, 3-State inputs	3.5/1.0	70 µA/0.6 mA
$\overline{OEAB}$	A-to-B Output Enable input (Active LOW)	1.0/1.0	20 µA/0.6 mA
$\overline{OEBA}$	B-to-A Output Enable input (Active LOW)	1.0/1.0	20 µA/0.6 mA
$\overline{EAB}$	A-to-B Enable input (Active LOW)	1.0/2.0	20 µA/1.2 mA
$\overline{EBA}$	B-to-A Enable input (Active LOW)	1.0/2.0	20 µA/1.2 mA
$\overline{LEAB}$	A-to-B Latch Enable input (Active LOW)	1.0/1.0	20 µA/0.6 mA
$\overline{LEBA}$	B-to-A Latch Enable input (Active LOW)	1.0/1.0	20 µA/0.6 mA
A0 - A7	Port A, 3-State outputs	150/40	3.0 mA/24 mA
B0 - B7	Port B, 3-State outputs	750/106.7	15 mA/64 mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 µA in the HIGH State and 0.6mA in the LOW state.

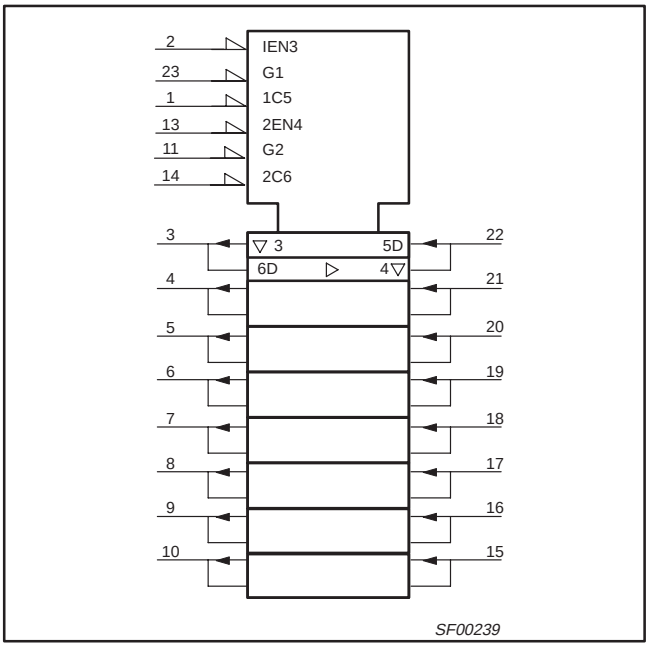
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

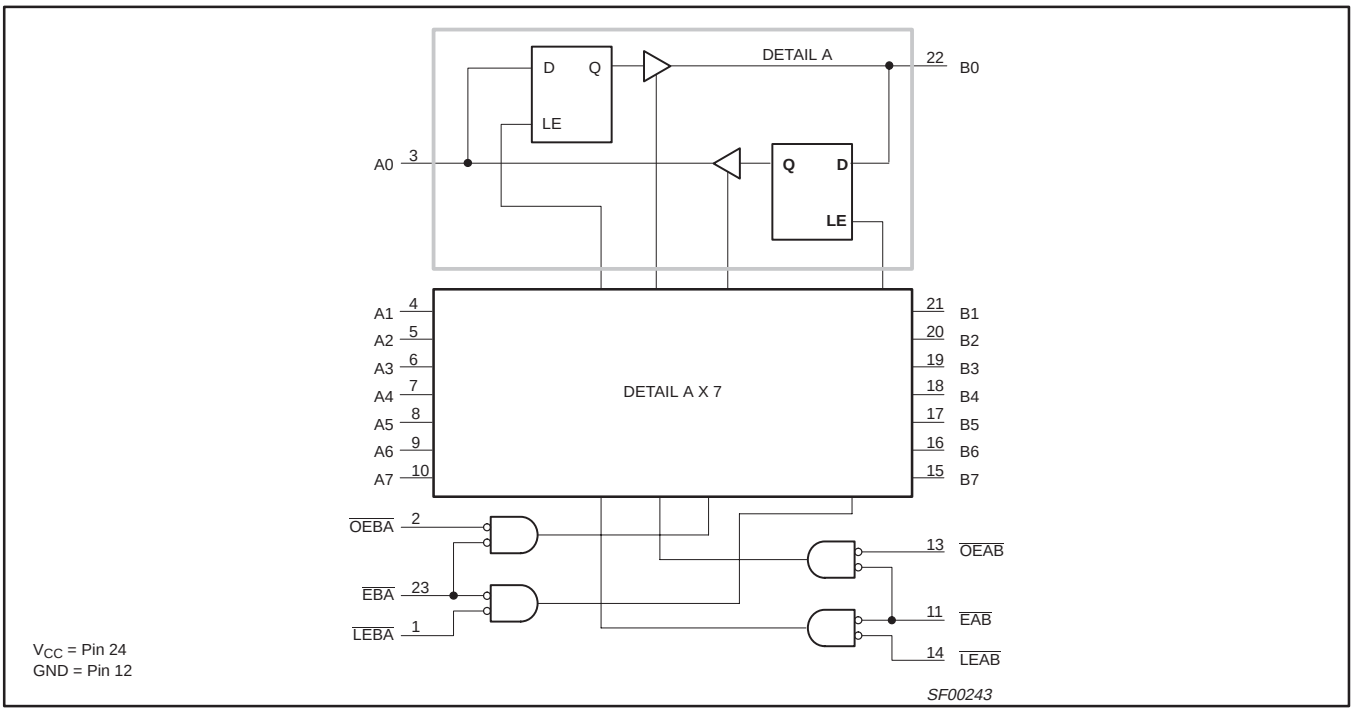


FUNCTION TABLE for 74F543

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disable + Latch
L	↑	L	I	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	I	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
I = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ = LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ XX = AB or BA
X = Don't care
NC = No change
Z = High-impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A0 - A7	48	mA
		B0 - B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
I_{IK}	Input clamp current		–	–	–18	mA
I_{OH}	HIGH-level output current	A0 - A7	–	–	–3	mA
		B0 - B7	–	–	–15	mA
I_{OL}	LOW-level output current	A0 - A7	–	–	24	mA
		B0 - B7	–	–	64	mA
T_{amb}	Operating free-air temperature range		–0	–	+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	HIGH-level output voltage	A0 - A7	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = –3 mA	± 10 % V_{CC}	2.4	–	–	V
					± 5 % V_{CC}	2.7	3.4	–	V
		B0 - B7		I_{OH} = –15 mA	± 10 % V_{CC}	2.0	–	–	V
					± 5 % V_{CC}	2.0	–	–	V
V_{OL}	LOW-level output voltage	A0 - A7	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 24 mA	± 10 % V_{CC}	–	0.35	0.50	V
					± 5 % V_{CC}	–	0.35	0.50	V
		B0 - B7		I_{OL} = 64 mA	± 10 % V_{CC}	–	–	0.55	V
					± 5 % V_{CC}	–	0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN; I_I = I_{IK}			–	–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$	V_{CC} = MAX; V_I = 7.0 V			–	–	100	µA
		Others	V_{CC} = 5.5 V; V_I = 5.5 V			–	–	1	mA
I_{IH}	HIGH-level input current		V_{CC} = MAX; V_I = 2.7 V			–	–	20	µA
I_{IL}	LOW-level input current	Others	V_{CC} = MAX; V_I = 0.5 V			–	–	–0.6	mA
		$\overline{EAB}$, $\overline{EBA}$				–	–	–1.2	mA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied		V_{CC}= MAX; V_O = 2.7 V			–	–	70	µA
I_{OZH} + I_{IL}	Off-state output current, LOW-level voltage applied		V_{CC}= MAX; V_O = 0. 5 V			–	–	–600	µA
I_{OS}	Short-circuit output current[3]	A0 - A7	V_{CC} = MAX			–60	–	–150	mA
		B0 - B7				–100	–	–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			–	70	105	mA
		I_{CCL}				–	95	135	mA
		I_{CCZ}				–	95	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

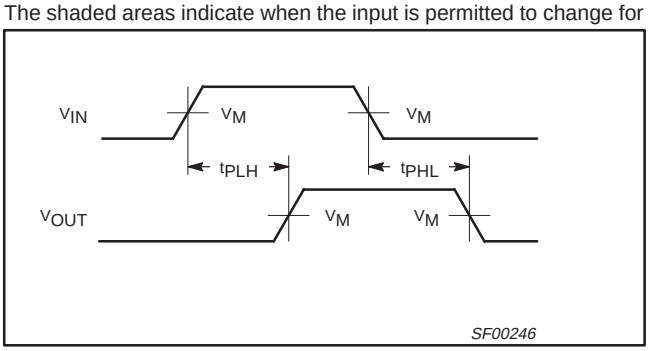
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = 5.0 V C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = 5.0 V ± 10 % C_L = 50pF; R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform 1	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 3 Waveform 4	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 3 Waveform 4	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 3 Waveform 4	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 3 Waveform 4	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS

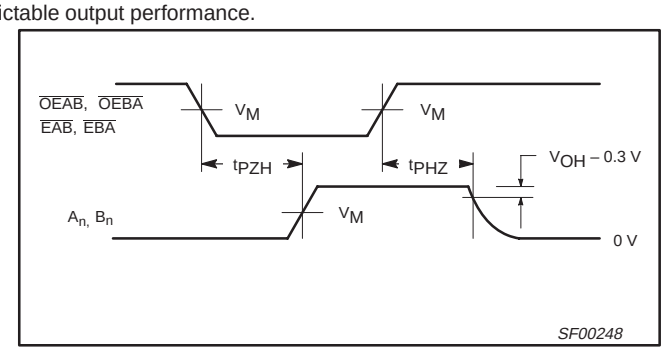
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			T_{amb} = +25 °C V_{CC} = 5.0 V C_L = 50 pF; R_L = 500 Ω		T_{amb} = 0 °C to +70 °C V_{CC} = 5.0 V ± 10 % C_L = 50 pF; R_L = 500 Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, HIGH or LOW A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 2	0.0 2.5	– –	0.0 3.0	– –	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 2	0.0 1.5	– –	0.0 2.0	– –	ns
t_s(H) t_s(L)	Setup time, HIGH or LOW A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 2	1.0 2.5	– –	1.5 3.0	– –	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 2	0.0 1.5	– –	0.0 2.0	– –	ns
t_w(L)	Latch enable pulse width, LOW	Waveform 2	4.0	–	4.5	–	ns

AC WAVEFORMS

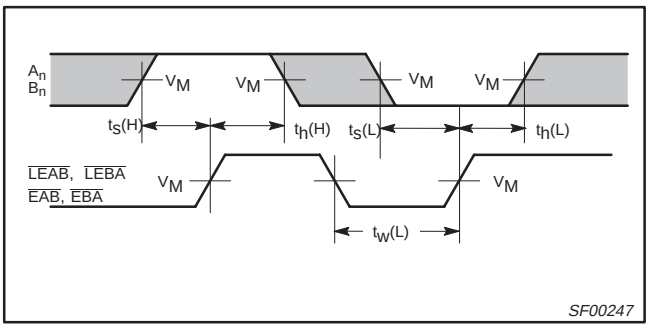
V_M = 1.5 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



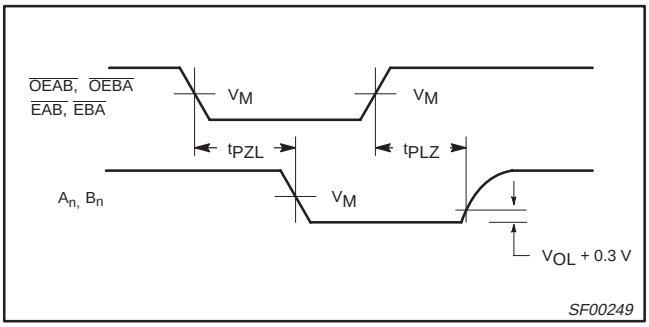
Waveform 1. Propagation delay for non-inverting outputs



Waveform 3. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

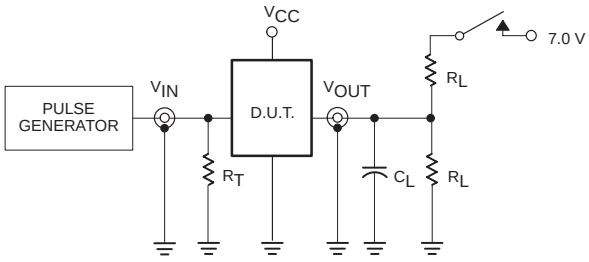


Waveform 2. Data Setup Time and Hold Times, and Latch Enable Pulse Width

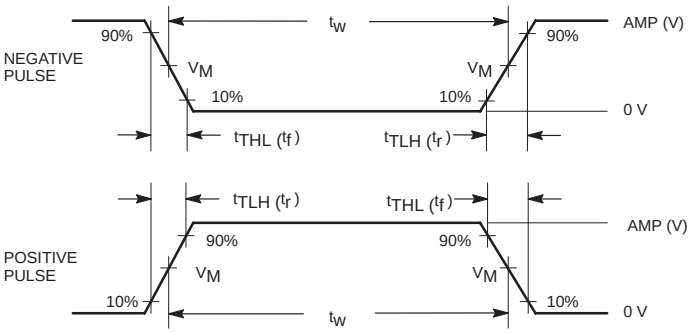


Waveform 4. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

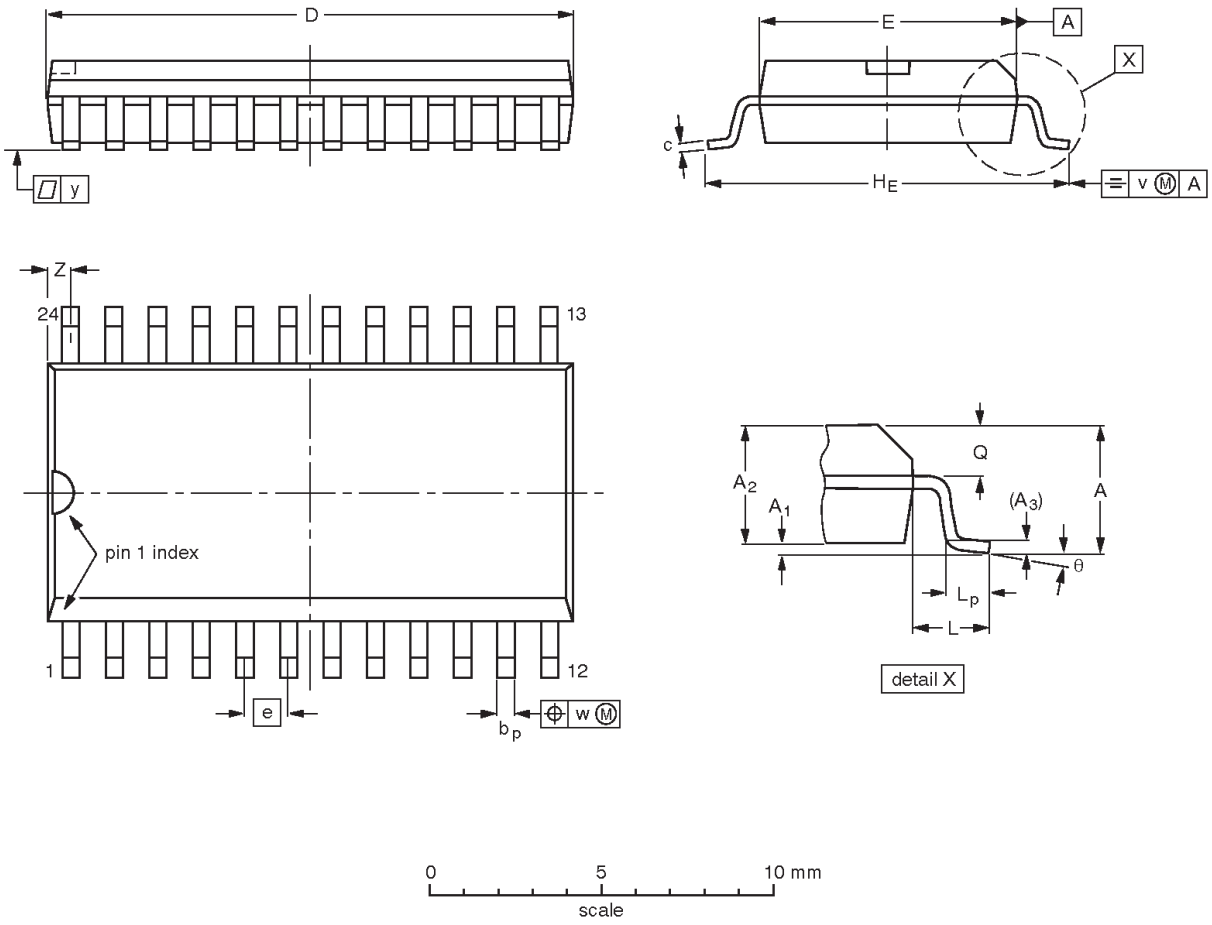
DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

SF00128

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

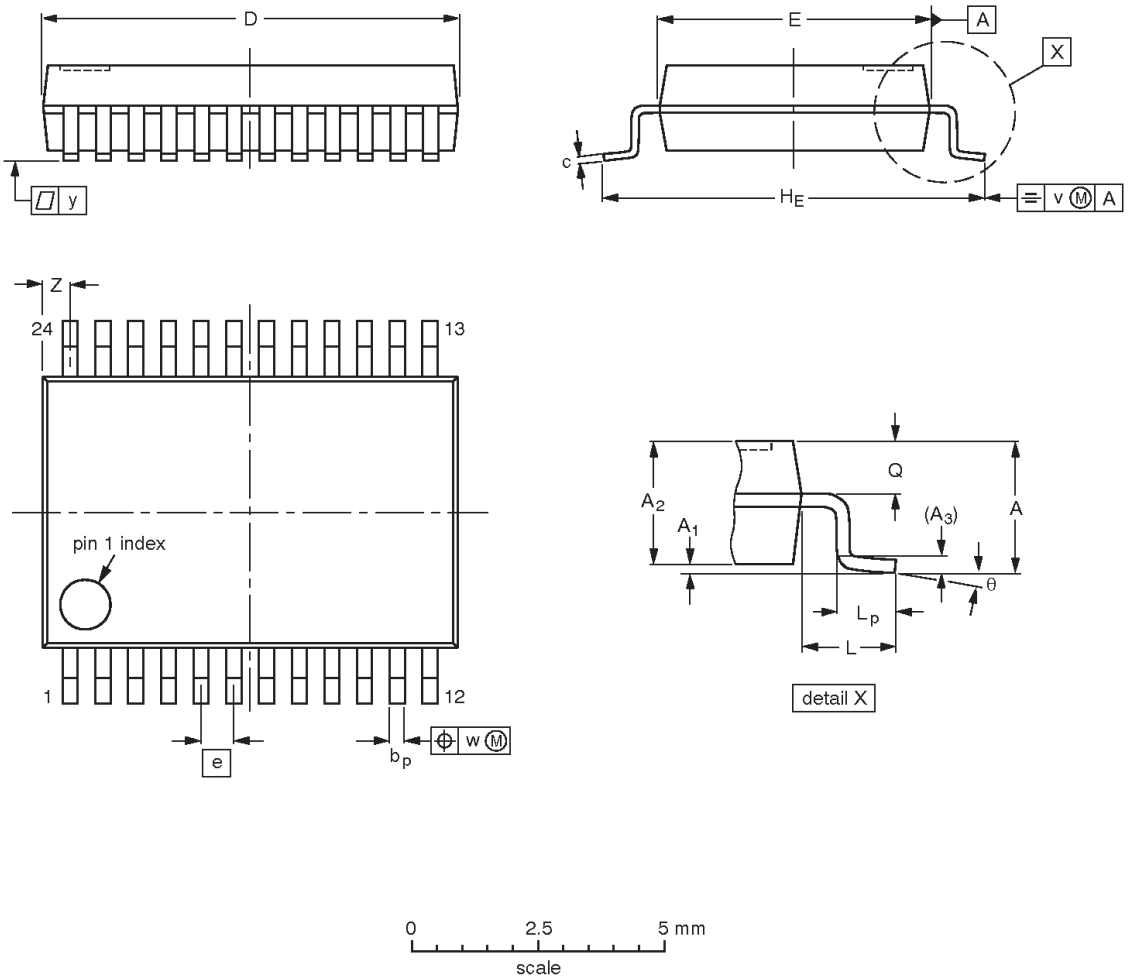
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

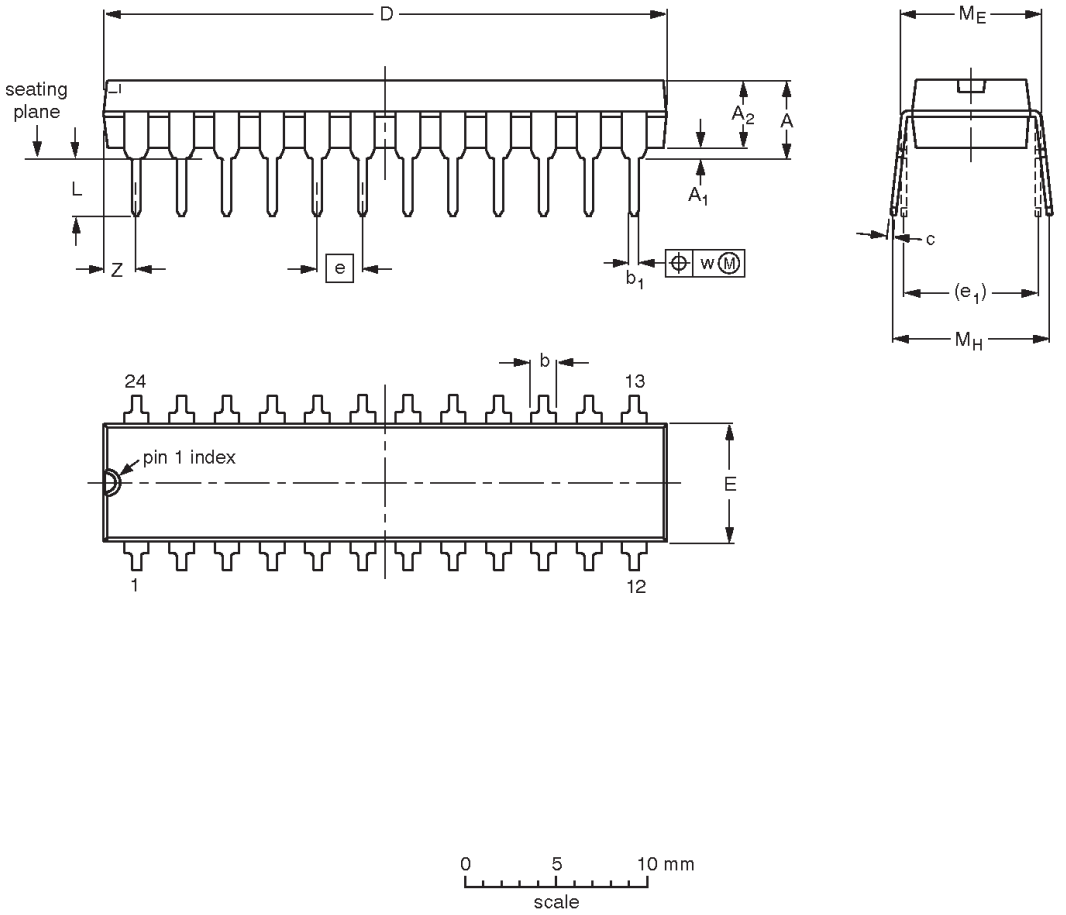
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				~~99-12-27~~ 03-03-12

REVISION HISTORY

Rev	Date	Description
_3	20040722	**Product data sheet (9397 750 13803).** **Replaces Product specification 74F543_544_1 of 1994 Dec 05 (9397 750 05135).** Modifications: • Remove part-type 74F544 and all its references. • Change Type number for SSOP24 package from “74F543DB” to “N74F543DB”.
_2	19941205	**Product specification (9397 750 05135). ECN 853-0874 14379 of 05 December 1994.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data sheet	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data sheet	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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