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# F DN8601

## N-Channel PowerTrench® MOSFET

### 100 V, 2.7 A, 109 mΩ

#### Features

- Max  $r_{DS(on)}$  = 109 mΩ at  $V_{GS} = 10$  V,  $I_D = 1.5$  A
- Max  $r_{DS(on)}$  = 175 mΩ at  $V_{GS} = 6$  V,  $I_D = 1.2$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

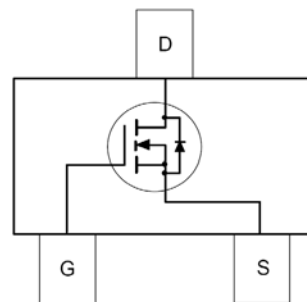
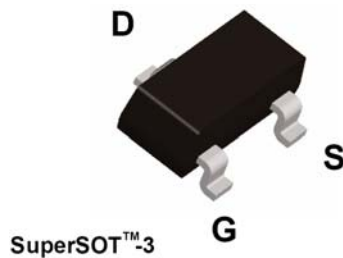


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

#### Applications

- Primary DC-DC Switch
- Load Switch



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	-Continuous (Note 1a)	2.7	A
	-Pulsed	12	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	13	mJ
$P_D$	Power Dissipation (Note 1a)	1.5	W
	Power Dissipation (Note 1b)	0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	80	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8601	F DN8601	SSOT-3	7"	8 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		68		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 1.5\ \text{A}$		85.4	109	m $\Omega$
		$V_{GS} = 6\ \text{V}, I_D = 1.2\ \text{A}$		117	175	
		$V_{GS} = 10\ \text{V}, I_D = 1.5\ \text{A}, T_J = 125\text{ }^\circ\text{C}$		143	183	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}, I_D = 1.5\ \text{A}$		8		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		156	210	pF
$C_{oss}$	Output Capacitance			47	65	pF
$C_{rss}$	Reverse Transfer Capacitance			2.7	5	pF
$R_g$	Gate Resistance			1.0		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 1.5\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		4.3	10	ns
$t_r$	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			7.8	16	ns
$t_f$	Fall Time			3.4	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 50\ \text{V},$ $I_D = 1.5\ \text{A}$	3	5	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$		1.8	3	nC
$Q_{gs}$	Gate to Source Gate Charge			0.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.8		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 1.5\ \text{A}$ (Note 2)		0.81	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 1.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		29	46	ns
$Q_{rr}$	Reverse Recovery Charge			15	27	nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



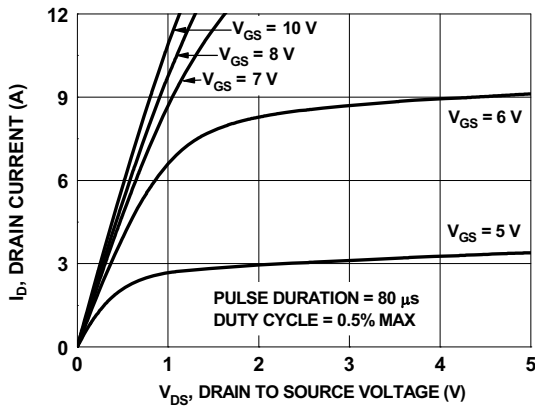
a)  $80\text{ }^\circ\text{C/W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper



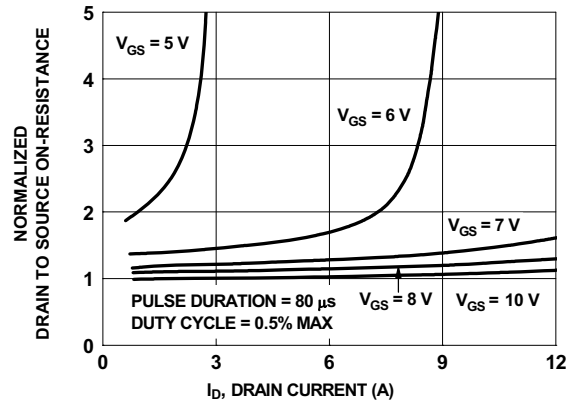
b)  $180\text{ }^\circ\text{C/W}$  when mounted on a minimum pad.

- Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\ \text{mH}, I_{AS} = 3\ \text{A}, V_{DD} = 100\ \text{V}, V_{GS} = 10\ \text{V}$ .

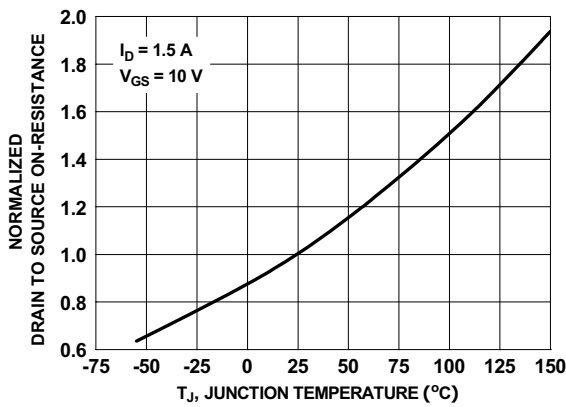
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



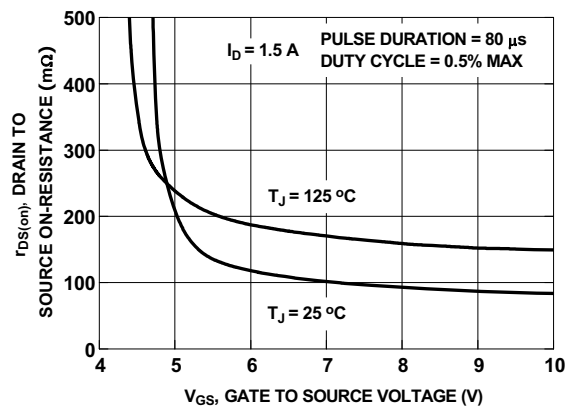
**Figure 1. On-Region Characteristics**



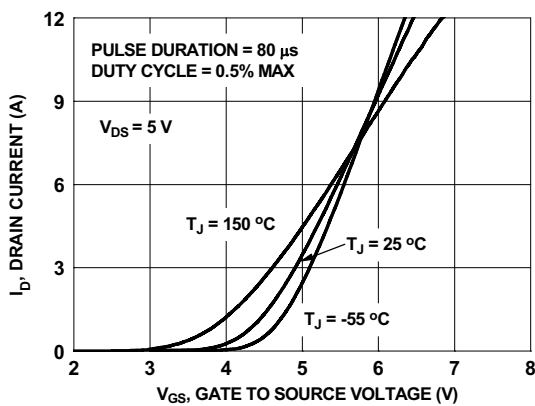
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



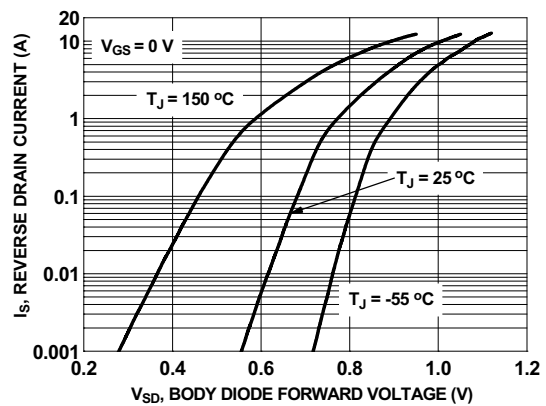
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

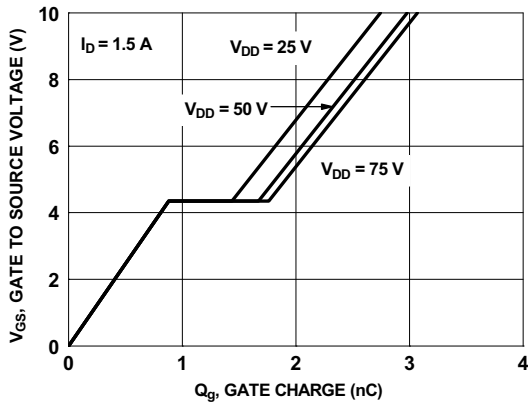


**Figure 5. Transfer Characteristics**

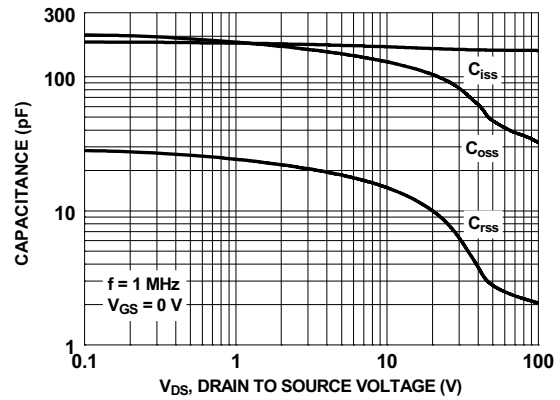


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

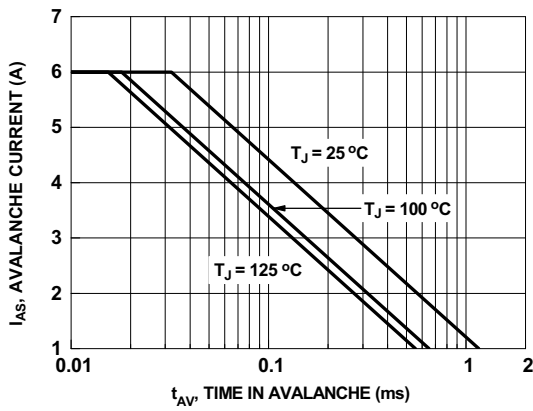
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



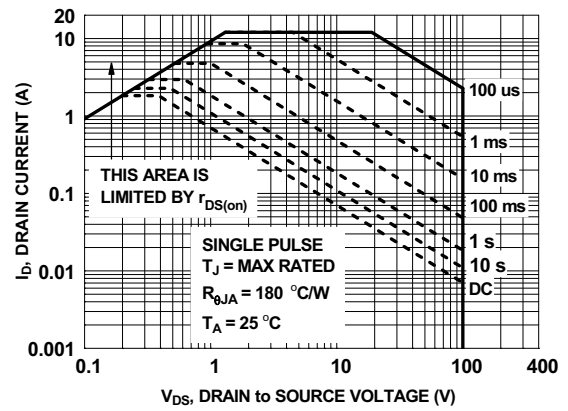
**Figure 7. Gate Charge Characteristics**



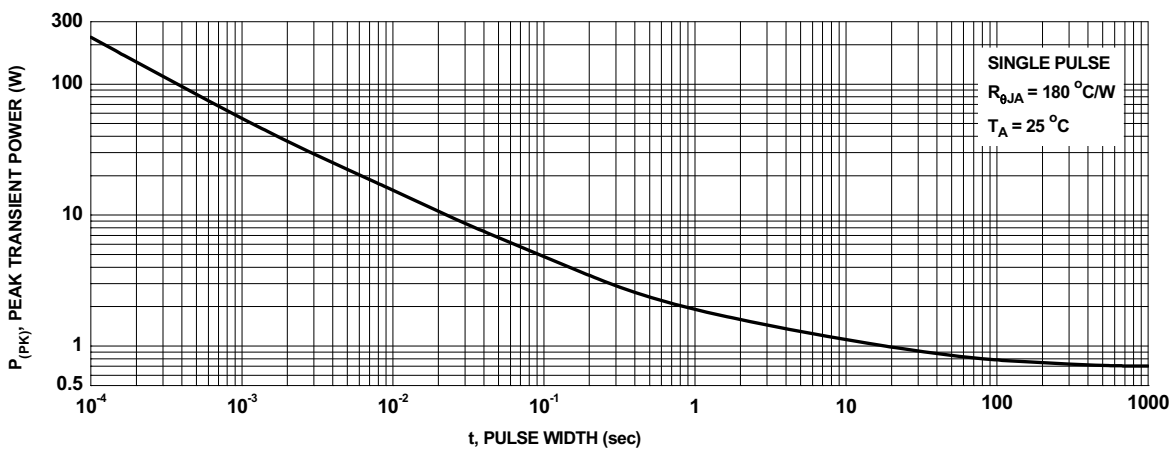
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**

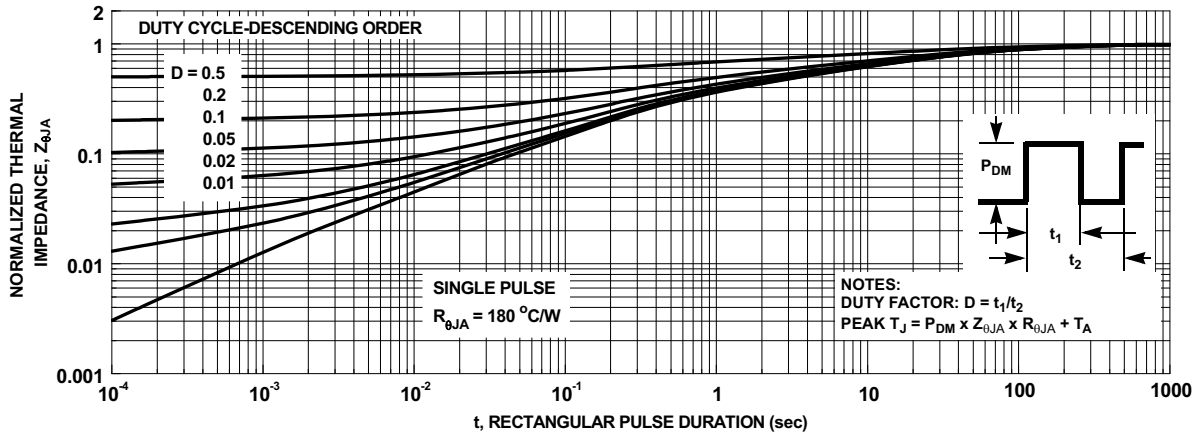


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**



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