PC PERIPHERAL CLOCK

ICS409

Description

The ICS409 is a cost-effective clock synthesizer developed to optimize component count for PC peripheral applications. The device supports a common, low cost 14.31818 MHz crystal using an on-chip crystal oscillator. The device locks all output frequencies to enhance system performance. By supporting common PC peripheral interface frequencies including dual 25 MHz and 40/80 MHz frequencies the clock lowers chip count enhancing system cost and reliability.

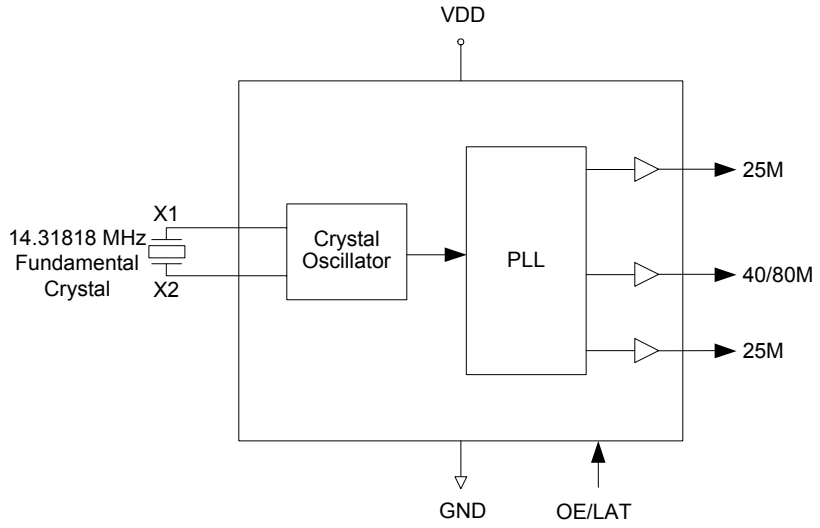
The ICS409 utilizes a low pin count 8-pin SOIC package to optimize board space.

IDT is a leader in low jitter and power consumer application clock sources. These devices are capable of supporting CCD, video, audio, USB, CPU, and other peripherals.

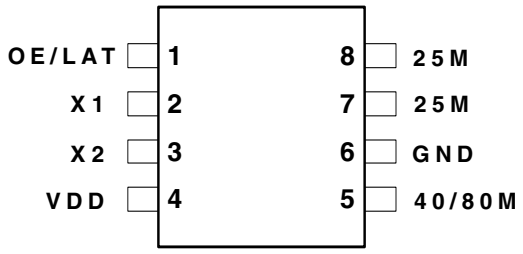
Features

- Pin compatible with FS6286-01
- Low operating voltage of 3.3V
- On-chip oscillator supports 14.31818 MHz crystal
- Fixed dual 25 MHz clocks for Ethernet
- 40/80 MHz selected on rising edge of OE/LAT pin
- Power consumption of 15 mA (typ)
- Duty cycle of 45 to 55%
- Packaged in 8-pin SOIC (Pb-free)

Block Diagram



Pin Assignment



8 Pin (150 mil) SOIC

40/80M Frequency Selection

40/80M (pin 5)	Output Freq
0	40M
1	80M

Note: See below for operations of frequency selection

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	OE/LAT	Input	Disables or latches 40/80 MHz output dependant on pin 5 level.
2	X1	Input	Crystal connection. Connect to 14.31818 MHz parallel mode crystal.
3	X2	Input	Crystal connection. Connect to 14.31818 MHz parallel mode crystal.
4	VDD	Power	Connect to voltage supply.
5	40/80M	Input/ Output	40M or 80M selection pin and clock output (see below for operation). Tri-state when OE/LAT is low.
6	GND	Power	Connect to ground.
7	25M	Output	25 MHz clock output.
8	25M	Output	25 MHz clock output.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

As with any high performance mixed-signal IC, the ICS409 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X1 to ground.

The value (in pF) of these crystal caps should equal (C_L -6pF)*2. In this equation, C_L= crystal load capacitance

in pF. Example: For a crystal with a 15 pF load capacitance, each crystal capacitor would be 18 pF [(15-6) x 2] = 18.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS409. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Selection of 40M/80M Clock

The 40/80M output clock is selected by a soft pull-up or pull-down on 40/80M pin (pin 5). A rising edge on OE/LAT latches in the high or low level on pin 5 which starts the appropriate frequency.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS409. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	175 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	°C
Power Supply Voltage (measured in respect to GND)	+3.00		+3.60	V

DC Electrical CharacteristicsDC Electrical Characteristics (continued)

VDD=3.3V ±10%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}		Vdd-0.5			V
Input Low Voltage	V_{IL}				0.5	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.8	V
Operating Supply Current	IDD	No load		15		mA
Short Circuit Current	I_{OS}	Each output		50		mA
Suggested Pull-up or Pull-down resistor on pin 5	R			10		kΩ

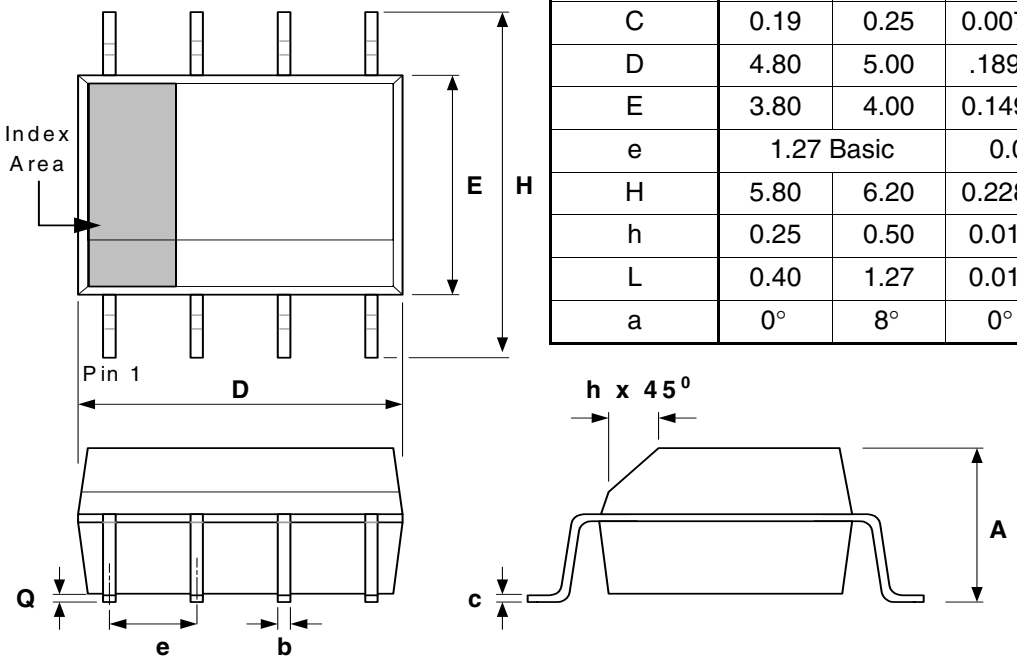
AC Electrical Characteristics

VDD = 3.3V ±10%, Ambient Temperature 0 to +70× C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				14.318		MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.8		ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.6		ns
Output Clock Duty Cycle		at VDD/2	45	50	55	%
Absolute Jitter, Short Term		variation from mean		±250		ps

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	1.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 Basic		0.050 Basic	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
a	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
409MLF	409MLF	Tubes	8-pin SOIC	0 to 70 °C
409MLFT	409MLF	Tape and Reel	8-pin SOIC	0 to 70 °C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
www.idt.com/go/clockhelp

Corporate Headquarters
Integrated Device Technology, Inc.
www.idt.com

www.IDT.com