PIC16C65A

PIC16C65A Rev. A Silicon Errata Sheet

The PIC16C65A (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30234**D**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C65A silicon.

1. Module: CCP (Compare Mode)

The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

TABLE 1: COMPARE OUTPUT LOW SWITCHING

CCP Mode CCPxM<3:0> =	I/O pin State	Change CCP to CCPxM<3:0> =	
		1001	1000
0xxx	H	L	L
	L	L	L
1000	H	H	—
	L	L	—
1001	H	—	L
	L	—	L
101x	H	L	L
	L	L	L
11xx	H	L	L
	L	L	L

Work around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low, when the compare condition occurs.

2. Module: CCP (Compare Mode)

The special event trigger of the Compare mode may not occur if both of the following conditions exist:

- An instruction, one cycle (T$_{CY}$) prior to a Timer1/Compare register match has literal data equal to the address of a CCP register being used. Specific cases include:

Unit	Register	Literal Data
CCP1	CCPR1L	15h
	CCPR1H	16h
	CCP1CON	17h

- An instruction in the same cycle as a Timer1/Compare register match has an MSb of '0'.

The interrupt for the compare event will still be generated, but no special event trigger will occur.

Work around

Use the Interrupt Service Routine instead of using the special event trigger to reset Timer1 (and start an A/D conversion, if applicable).

3. Module: SSP Module (I^{2}C™ mode)

If the bus is active when the I^{2}C mode is enabled, and the next 8 bits of data on the bus match the address of the device, then the SSP module will generate an Acknowledge pulse.
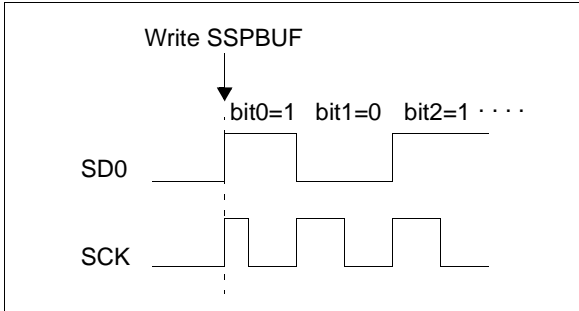
Work around

Before enabling the I^{2}C mode, ensure that the bus is not active.

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4. Module: SSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2

Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit, and then turn Timer2 back on. Refer to Example 1 for sample code.

EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK PULSE

```
      BSF    STATUS, RP0   ;Bank 1
LOOP BTFSS SSPSTAT, BF     ;Data received?
                           ;(Xmit complete?)
      GOTO   LOOP          ;No
      BCF    STATUS, RP0   ;Bank 0
      MOVF   SSPBUF, W     ;W = SSPBUF
      MOVWF  RXDATA        ;Save in user RAM
      MOVF   TXDATA, W     ;W = TXDATA
      BCF    T2CON, TMR2ON ;Timer2 off
      CLR    TMR2          ;Clear Timer2
      MOVWF  SSPBUF        ;Xmit New data
      BSF    T2CON, TMR2ON ;Timer2 on
```

5. Module: Timer0

The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).

Work around

Follow the following sequence:

a) Read the 8-bit TMR0 register into the W register
b) Clear the TMR0 register
c) Assign WDT postscaler to Timer0
d) Write W register to TMR0

6. Module: Timer1

The Timer1 value may unexpectedly increment if either the TMR1H, or the TMR1L register is written. If Timer1 is ON and then turned OFF, performing any write instruction with TMR1H as the destination, may cause TMR1L to increment.

EXAMPLE 2: TMR1L INCREMENT (CASE 1)

```
BSF T1CON, TMR1ON
           :
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:
    TMR1H:TMR1L = 3F:00
TMR1 value after MOVF instruction:
    TMR1H:TMR1L = 3F:01

EXAMPLE 3: TMR1L INCREMENT (CASE 2)

```
BSF T1CON, TMR1ON
           :
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:
    TMR1H:TMR1L = FF:FF
TMR1 value after MOVF instruction:
    TMR1H:TMR1L = FF:00

If Timer1 is ON and then turned OFF when TMR1H:TMR1L = xx:FF, performing any write instruction with TMR1L as the destination, may cause TMR1H to increment.

EXAMPLE 4: TMR1H INCREMENT

```
BSF T1CON, TMR1ON
BCF T1CON, TMR1ON
CLRF TMR1L
```

TMR1 value before CLRF instruction:
    TMR1H:TMR1L = FF:FF
TMR1 value after CLRF instruction:
    TMR1H:TMR1L = 00:00
(TMR1IF is **not** set.)

Work around

To preserve Timer1 register values:

a) Read Timer1 register values into "shadow" registers.
b) Perform any write instruction(s) on the shadow registers.
c) Write the shadow register values back into the Timer1 registers.

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7. Module: USART

When the USART (SCI) is configured in Asynchronous mode with the BRGH bit set, a high number of receive errors may be experienced. For asynchronous receive operations, it is recommended that the USART be configured with the BRGH bit cleared.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30234**D**), the following clarifications and corrections should be noted.

1. Module: I/O Ports

The specification for the High Voltage Open Drain I/O (parameter D150, the RA4 pin) cannot be met without possible long term reliability issues on that I/O pin. If a high voltage drive is required, use an external transistor that can support the required voltage. The new value is shown in Table 1.

TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D150	V_{OD}	RA4 Open Drain High Voltage	—	—	10	—	—	14	V

2. Module: SSP (SPI Mode Timing Specifications)

The SPI interface timings (parameters 71, 71A, 72, 72A, 73, and 73A) have been modified. The new values are shown in Table 2.

TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
71	T_{scH}	SCK input high time (Slave mode)	Continuous	1.25 T_{CY} + 30 ns	—	—	T_{CY} + 20 ns	—	—	ns
71A			Single Byte[1]	40	—	—	N.A.			ns
72	T_{scL}	SCK input low time (Slave mode)	Continuous	1.25 T_{CY} + 30 ns	—	—	T_{CY} + 20 ns	—	—	ns
72A			Single Byte[1]	40	—	—	N.A.			ns
73A	T_{B2B}	Last clock edge of the Byte1 to 1st clock edge of the Byte2[1]		1.5 T_{CY} + 40 ns	—	—	N.A.			ns

* This parameter is characterized but not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

3. Module: Timer1

The operation of Timer1 needs some clarification when the timer registers are written and the TMR1ON bit is set.

The internal clock signal, that is the input to the TMR1 prescaler, affects the incrementing of Timer1 (TMR1H:TMR1L registers and the Timer1 prescaler). When the Timer1 registers are NOT written, the Timer1 will increment on the rising edge of the TMR1 increment clock.

When the TMR1H and/or TMR1L registers are written while this clock is high, TMR1 will increment on the next rising edge of this clock.

When the TMR1H and/or TMR1L registers are written while this clock is low, TMR1 will not increment on the next rising edge of this clock, but must first have a falling clock and the rising clock for TMR1 to increment.

Figure 1 shows the two cases of writes to the TMR1H and/or TMR1L registers. Due to the V_{IH} and V_{IL} thresholds on the oscillator/clock pins, external Timer1 oscillator components, and external clock frequency, the Timer1 increment clock may not be of a 50% duty cycle.

The TMR1 increment clock is out of phase of the T1OSO/T1CKI pin by a small propagation delay.

FIGURE 1: WRITES TO TIMER1 (EXTERNAL CLOCK/OSCILLATOR MODE)
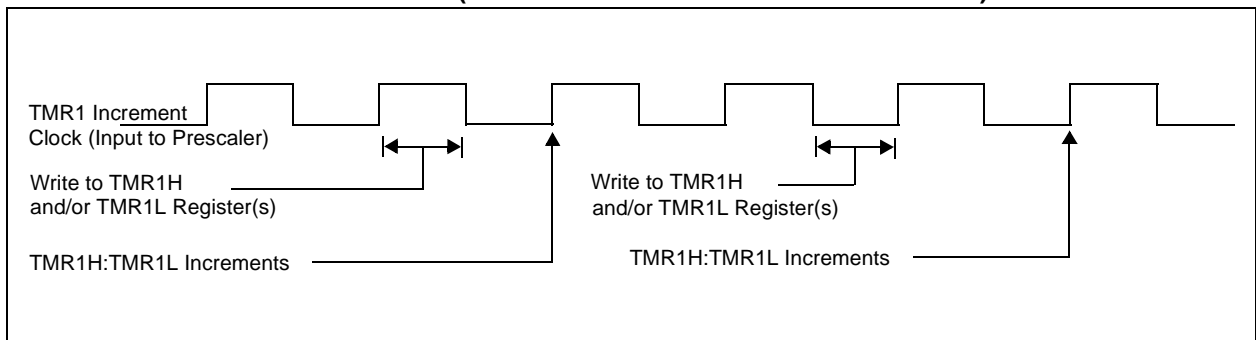
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4. Module: RC Oscillator

The table for RC Oscillator Frequencies in the Device Characterization section of the Data Sheet is incorrect. The correct characterization information is shown in Table 3.

TABLE 3: RC OSCILLATOR FREQUENCIES CHARACTERIZATION CHANGES FROM DATA SHEET

C_{EXT}	R_{EXT}	Correct Characterization Data		Current Data Sheet Values	
		Average	% Variation	Average	% Variation
22 pF	5.1 K	3.55 MHz	± 9.63%	4.12 MHz	± 1.4%
	10 K	1.99 MHz	± 10.53%	2.35 MHz	± 1.4%
	100 K	221.9 kHz	± 12.10%	268 kHz	± 1.1%
100 pF	3.3 K	1.77 MHz	± 10.67%	1.80 MHz	± 1.0%
	5.1 K	1.22 MHz	± 10.41%	1.27 MHz	± 1.0%
	10 K	669.4 kHz	± 10.92%	688 kHz	± 1.2%
	100 K	71.5 kHz	± 11.21%	77.2 kHz	± 1.0%
330 pF	3.3 K	625.1 kHz	± 10.68%	707 kHz	± 1.4%
	5.1 K	428.5 kHz	± 10.96%	501 kHz	± 1.2%
	10 K	231.9 kHz	± 11.32%	269 kHz	± 1.6%
	100 K	24.4 kHz	± 12.93%	28.3 kHz	± 1.1%

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from the average value for V_{DD} = 5V.

5. Module: Brown-Out Reset (BOR)

The levels specified for the BOR module thresholds (parameter D005) have changed. The new values are shown in Table 4.

TABLE 4: MINIMUM AND MAXIMUM BOR RESET VOLTAGES

| Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D005	V_{BOR}	Brown-out Reset Voltage	3.65	—	4.35	3.70	—	4.30	V

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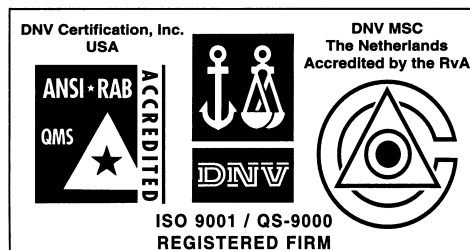
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