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Kind regards,

Team Nexperia

# PHN203

## Dual N-channel TrenchMOS logic level FET

Rev. 05 — 27 April 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Lithium-ion battery applications

### 1.4 Quick reference data

Table 1. Quick reference data

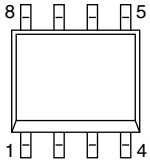
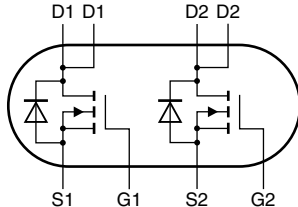
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{amb} = 25\text{ °C}$ ; pulsed; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	6.3	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$ ; pulsed; see <a href="#">Figure 2</a>	[1]	-	2	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 7\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	24	30	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 7\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>	-	3	-	nC

[1] Single device conducting.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>SOT96-1 (SO8)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHN203	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

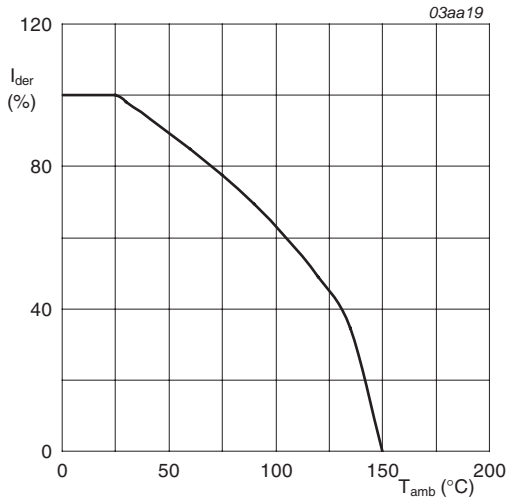
## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

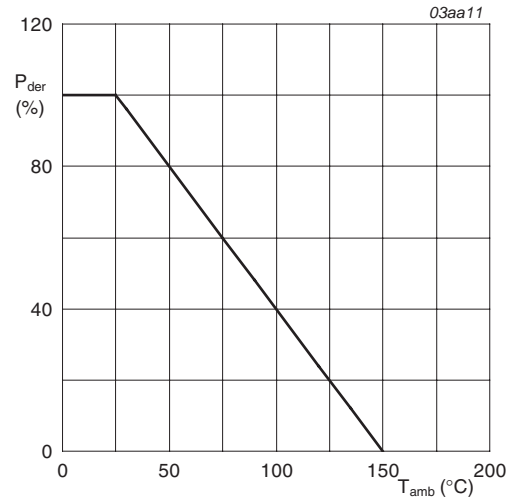
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \leq 150\text{ °C}$ ; $T_j \geq 25\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	-	30	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$T_{amb} = 70\text{ °C}$ ; pulsed; see <a href="#">Figure 1</a>	[1]	-	5	A
		$T_{amb} = 25\text{ °C}$ ; pulsed; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	6.3	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{amb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	[1]	-	18	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$ ; pulsed; see <a href="#">Figure 2</a>	[1]	-	2	W
$T_{stg}$	storage temperature		-55	-	150	°C
$T_j$	junction temperature		-55	-	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$ ; pulsed	[1]	-	2	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{amb} = 25\text{ °C}$	[1]	-	4.1	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 8.7\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; unclamped; $t_p = 0.2\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	-	37.8	mJ

[1] Single device conducting.



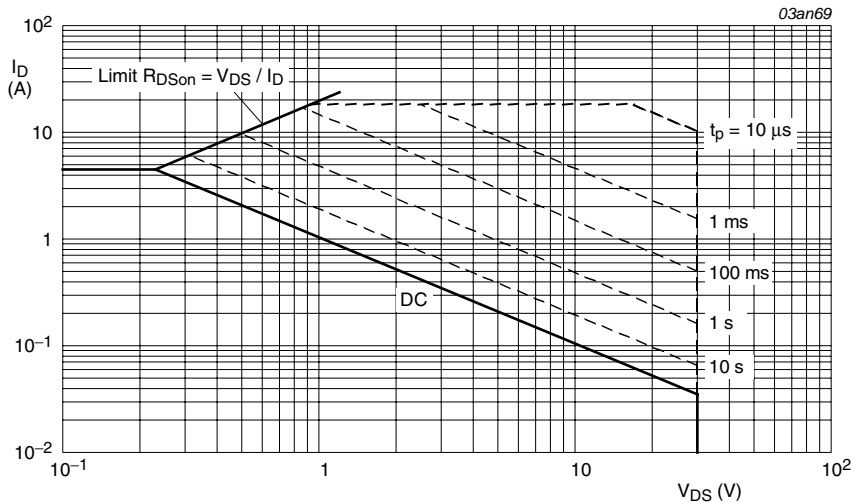
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of ambient temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of ambient temperature



$T_{amb} = 25^\circ C; I_{DM}$  is single pulse;  $V_{GS} = 10V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; see <a href="#">Figure 4</a>	-	-	62.5	K/W

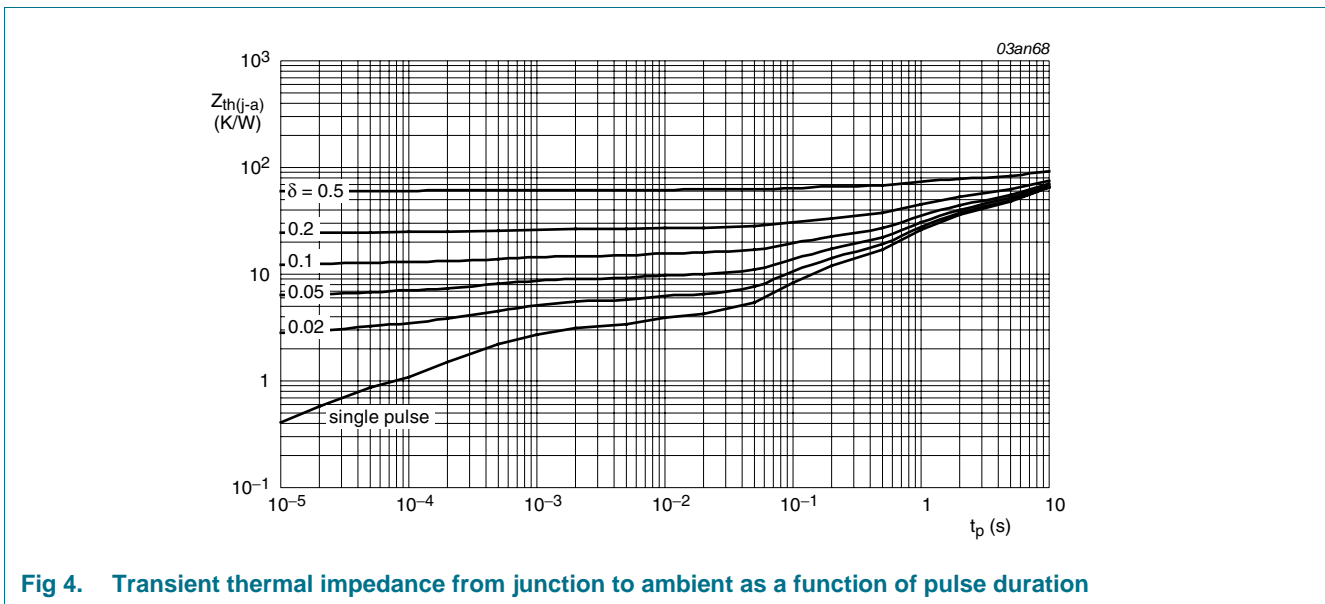
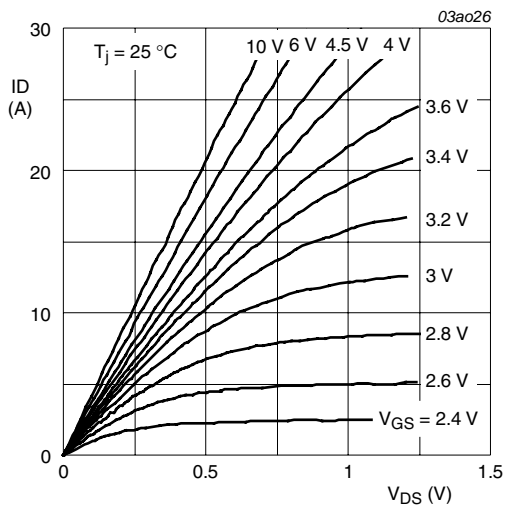


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration

## 6. Characteristics

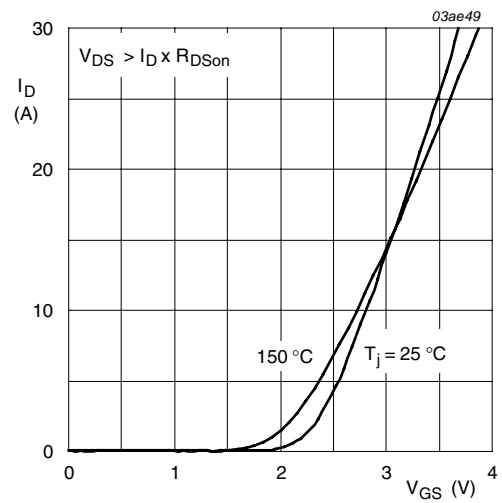
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	-	-	2.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 7 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	24	30	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 3.5 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	30	55	m $\Omega$
		$V_{GS} = 10 V; I_D = 7 A; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	40.8	51	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 7 A; V_{DS} = 15 V; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	14.6	-	nC
$Q_{GS}$	gate-source charge		-	2	-	nC
$Q_{GD}$	gate-drain charge		-	3	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	560	-	pF
$C_{oss}$	output capacitance		-	125	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	85	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25 V; R_L = 25 \text{ } \Omega; V_{GS} = 10 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	5	-	ns
$t_r$	rise time		-	6	-	ns
$t_{d(off)}$	turn-off delay time		-	21	-	ns
$t_f$	fall time		-	11	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.25 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	0.75	1	V
$t_{rr}$	reverse recovery time	$I_S = 2 A; di_S/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 \text{ }^\circ C$	-	30	-	ns



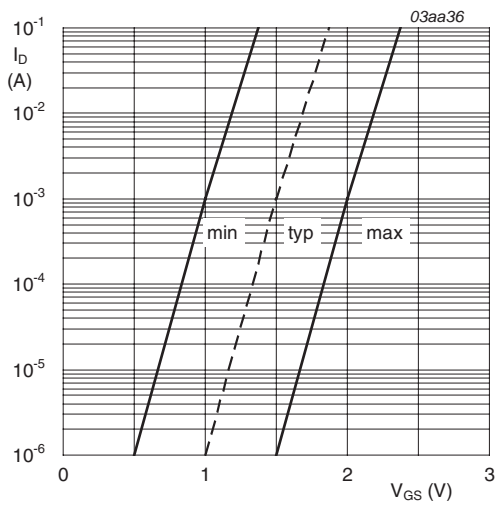
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical value



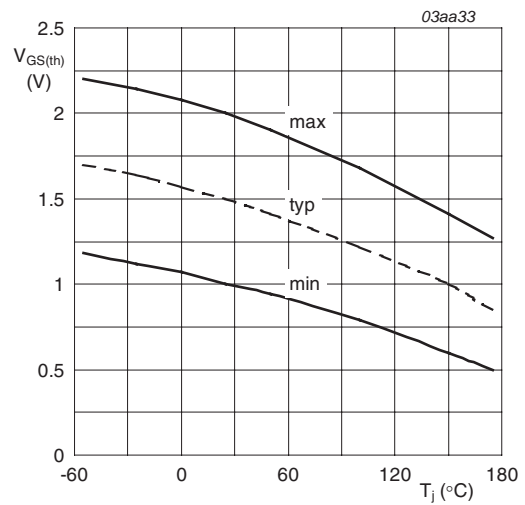
$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



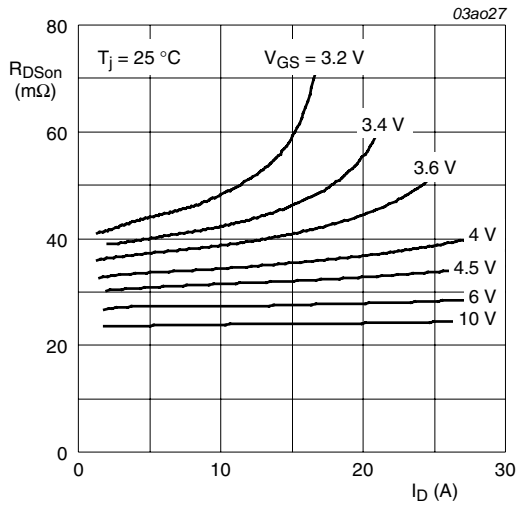
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



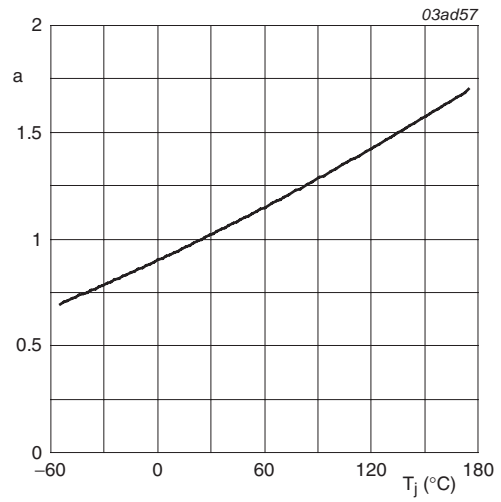
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



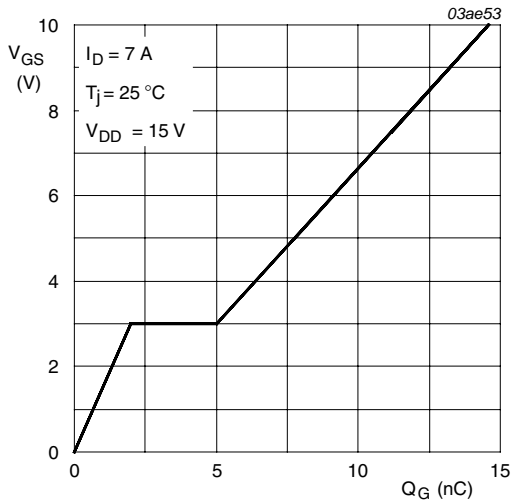
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



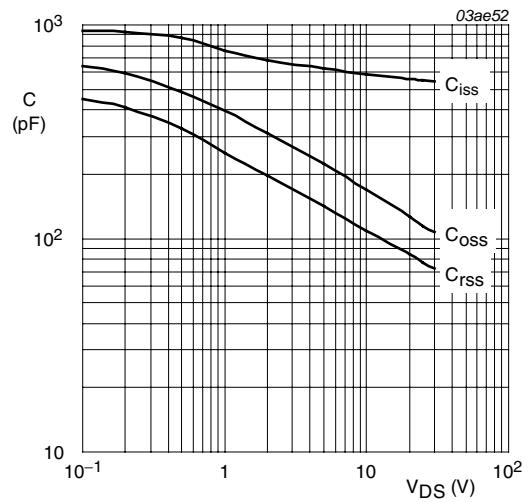
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 7\text{ A}; V_{DS} = 15\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



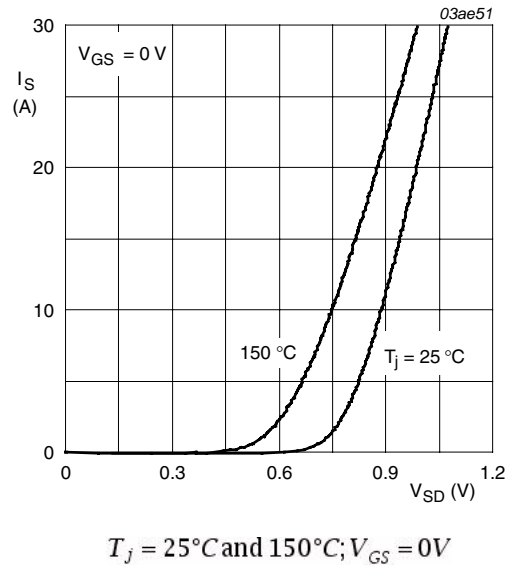


Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

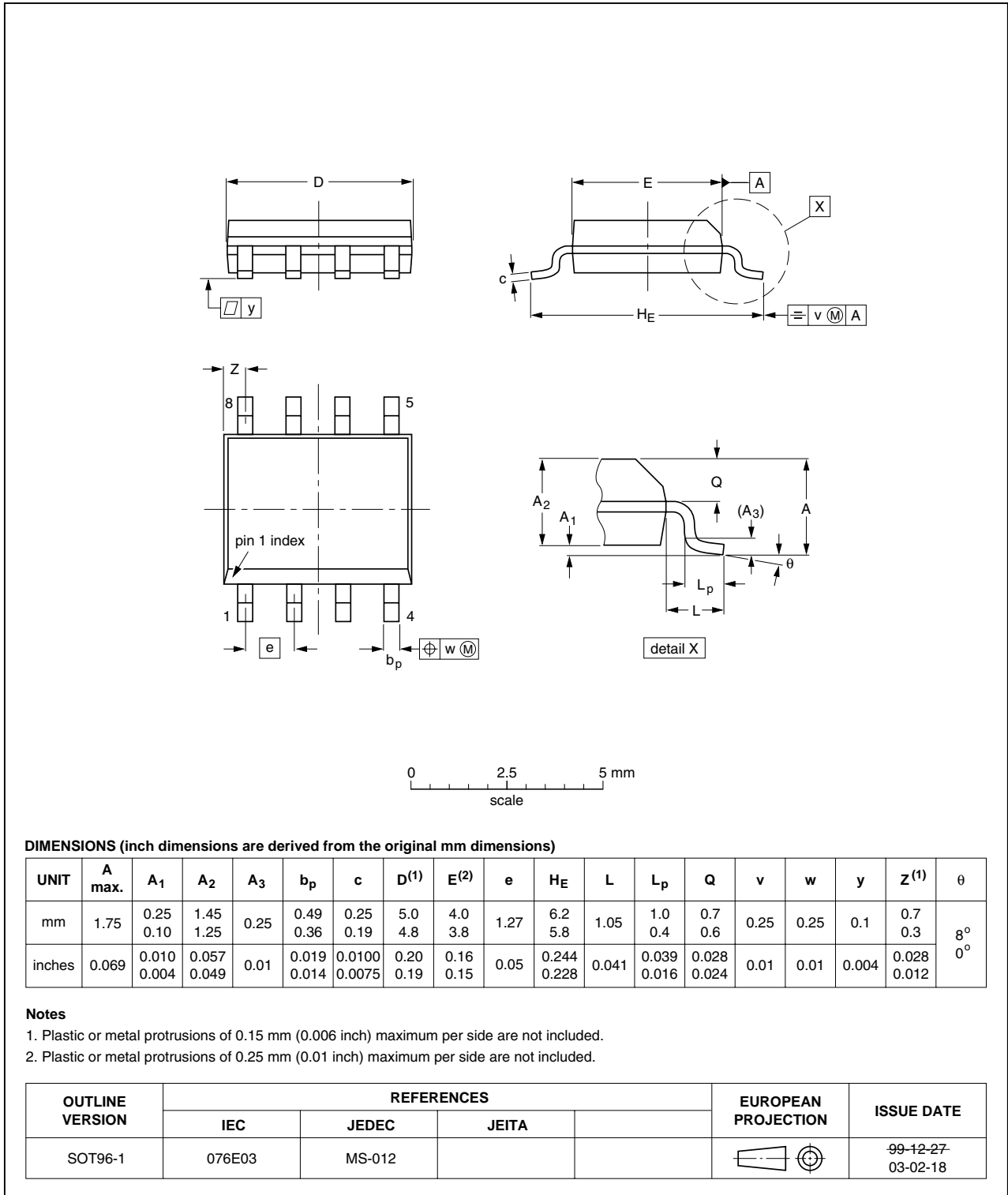


Fig 14. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHN203 _5	20100427	Product data sheet	-	PHN203 _4
Modifications:	• Various changes to content.			
PHN203 _4	20091208	Product data sheet	-	PHN203-03
PHN203 -03	20040126	Product data	-	PHN203 _2
PHN203 _2	19990101	Product specification	-	PHN203 _1
PHN203 _1	19980204	Objective specification	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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