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Team Nexperia

IP4352CX24

9-channel SD memory card interface filter with ESD protection to IEC 61000-4-2 level 4

Rev. 02 — 3 May 2010 Product data sheet

1. Product profile

1.1 General description

The IP4352CX24 is a diode array designed to provide protection to downstream components against ElectroStatic Discharge (ESD) voltages as high as 15 kV.

The IP4352CX24 integrates 9 pairs of rail-to-rail diodes, 15 resistors and 12 Zener diodes in a single Wafer-Level Chip-Scale Package (WLCSP) using monolithic silicon semiconductor technology.

These features make the IP4352CX24 ideal for applications requiring miniaturized components, such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- Pb-free, RoHS compliant, free of halogen and antimony (Dark Green compliant)
- All SD memory card channels have integrated ESD protection EMI and RF filters
- ESD protection up to 15 kV at output terminals on 9 channels
- Integrated EMI and RF filters with pull-up resistors on 5 channels
- Integrated EMI and RF filters on 4 channels
- SD card power supply protection
- WLCSP with 0.4 mm pitch
- Write protection with integrated card detect biasing resistor
- Supports electrical card detection
- Also available with different filter behavior and the same footprint as IP4350CX24

1.3 Applications

- SD memory card interfaces in cellular and PCS mobile handsets
- DECT handsets
- Digital still and video cameras
- Media players
- Card readers

2. Pinning information

2.1 Pinning

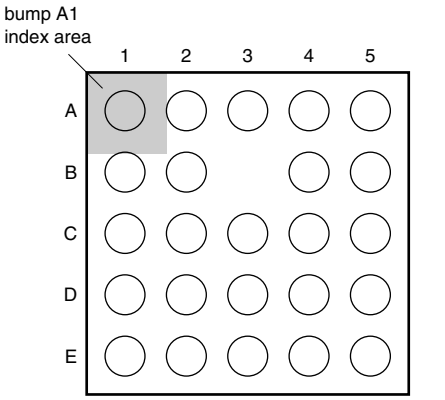


Fig 1. Pin configuration IP4352CX24

Table 1. Pinning

Pin	Description
A1	DATA2: data line 2
A2	DATA3: data line 3
A3	GND_H: ground 1
A4	SDDATA2: secure digital data 2
A5	SDDATA3: secure digital data 3
B1	CD: card detect
B2	CMD: command
B3	not connected
B4	SDCD: secure digital card detect
B5	SDCMD: secure digital command
C1	DAT3_PD: data 3 pull-down
C2	WP: write protect
C3	DAT3_PU: data 3 pull-up
C4	SDWP: secure digital write protect
C5	VSD: supply voltage
D1	WP+CD: write protect and card detect
D2	CLK: clock
D3	GND_C: ground 2
D4	SDWP+CD: secure digital write protect and card detect
D5	SDCLK: secure digital clock
E1	DATA1: data line 1

Table 1. Pinning *…continued*

Pin	Description
E2	DATA0: data line 0
E3	GND_C: ground 3
E4	SDDATA1: secure digital data 1
E5	SDDATA0: secure digital data 0

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4352CX24/LF	WLCSP24	wafer level chip-size package; 24 bumps (5 × 5 - B3)	IP4352CX24

4. Functional diagram

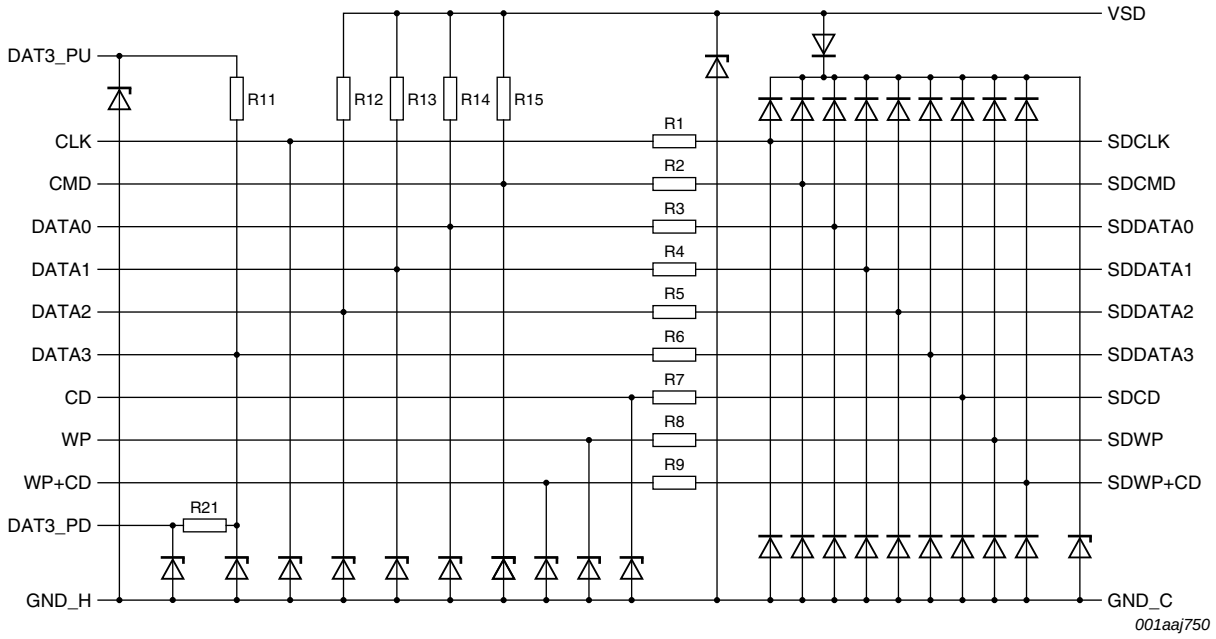


Fig 2. Schematic diagram IP4352CX24

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			–0.5	+5.0	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 level 4; output pins A4, A5, B4, B5, C4, C5, D4, D5, E4, E5; pins A3, D3 and E3 connected to ground				
		contact discharge	[1]	–8	+8	kV
		air discharge		–15	+15	kV
		IEC 61000-4-2 level 1; all other pins; pins A3, D3 and E3 connected to ground				
		contact discharge		–2	+2	kV
		air discharge		–2	+2	kV
P_{ch}	channel power dissipation	continuous power; T_{amb} = 70 °C		-	25	mW
P_{tot}	total power dissipation	continuous power; T_{amb} = 70 °C		-	100	mW
T_{stg}	storage temperature			–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum		-	260	°C
T_{amb}	ambient temperature			–30	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	R1 to R9 ± 20 %		32	40	48	Ω
		R11 to R14 ± 30 %		35	50	65	kΩ
		R15 ± 30 %		10.5	15	19.5	kΩ
		R21 ± 30 %		329	470	611	kΩ
C_{ch}	channel capacitance	$V_{bias(DC)}$ = 0 V; f = 1 MHz; pin DAT3_PU = 0 V; pin DAT3_PD = 0 V; pin VSD = 0 V					
		SD card to I/O interface	[1]	-	-	20	pF
		pins DAT3_PD, DAT3_PU and VSD	[1]	-	30	-	pF
V_{BR}	breakdown voltage	I_I = 1 mA		6	-	-	V
I_{LR}	reverse leakage current	per channel; V_I = 3 V		-	-	100	nA

[1] Guaranteed by design.

Table 5. Frequency response

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	all channels; R_{gen} = 50 Ω; R_L = 50 Ω				
		f < 400 MHz	-	-	9	dB
		400 MHz < f < 800 MHz	9	-	-	dB
		800 MHz < f < 2.5 GHz	13	-	-	dB
		2.5 GHz < f < 6 GHz	28	32	-	dB

Table 6. Time domain response

Measured using source with 0 V to 3 V steps and 20 % to 70 % LOW-to-HIGH limits; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High speed R_{gen} = 50 Ω; t_r = t_f = 2 ns[1]						
t_r	rise time	R_L = 20 pF || 100 kΩ	-	3.2	3.7	ns
		R_L = 40 pF || 100 kΩ	-	4.4	6	ns
t_f	fall time	R_L = 20 pF || 100 kΩ	-	3.3	4.3	ns
		R_L = 40 pF || 100 kΩ	-	5.5	7.5	ns

[1] Performed on all high speed lines (channels including R1 to R9, see Figure 2).

7. Application information

7.1 Insertion loss

The insertion loss was measured with a test PCB utilizing laser-drilled micro-via holes which connect the PCB ground plane to the ground pins.

The configuration for measuring insertion loss in a 50 Ω system is shown in Figure 3.

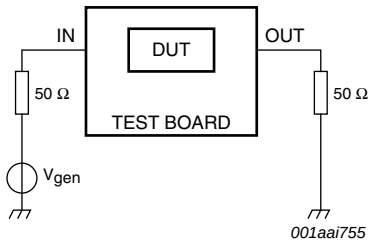
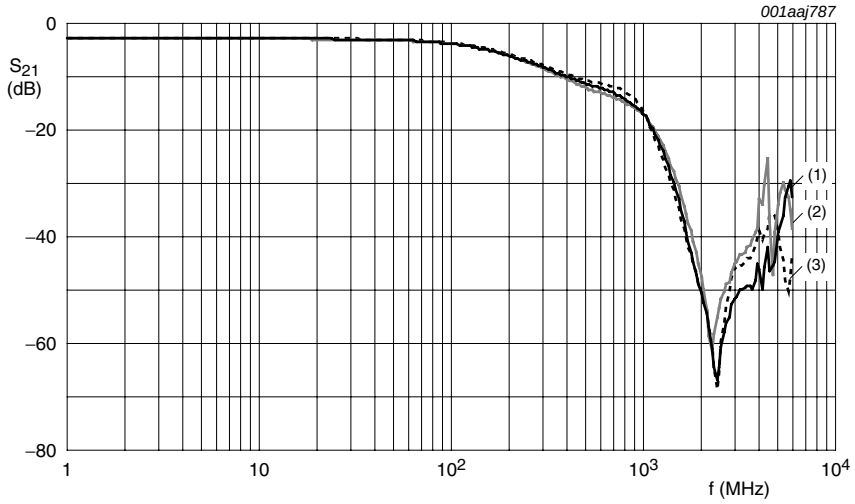


Fig 3. Frequency response measurement configuration

The frequency response curves measured on pins A1 and A4, E1 and E4 and C2 and C4 at frequencies up to 3 GHz are shown in Figure 4.



(1) Pin A1 to A4.
(2) Pin E1 to E4.
(3) Pin C2 to C4.

Fig 4. Measured insertion loss magnitudes

7.2 Crosstalk

The crosstalk between adjacent channels within the IP4352CX24 for different channel pairs was measured in a 50 Ω NetWork Analyzer (NWA) system.

The configuration for measuring crosstalk in a 50 Ω system is shown in Figure 5.

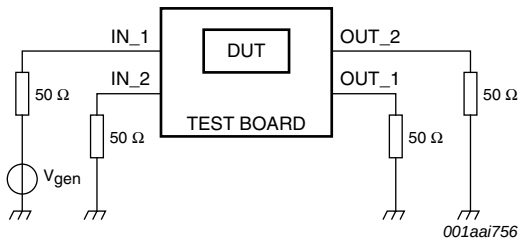
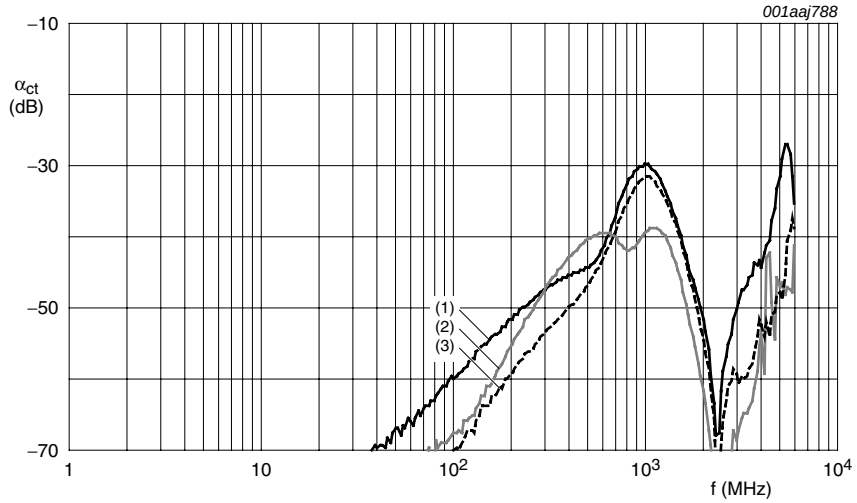


Fig 5. Crosstalk measurement configuration

The crosstalk measured for five different pairs of channels is shown in Figure 6. In all cases, all unused connections are terminated with 50 Ω to ground.



(1) Pins A1 and B4.

(2) Pins A1 and E4.

(3) Pins A2 and B5.

Fig 6. Measured crosstalk between different channels

8. Package outline

WLCSP24: wafer level chip-size package; 24 bumps (5 x 5 - B3)

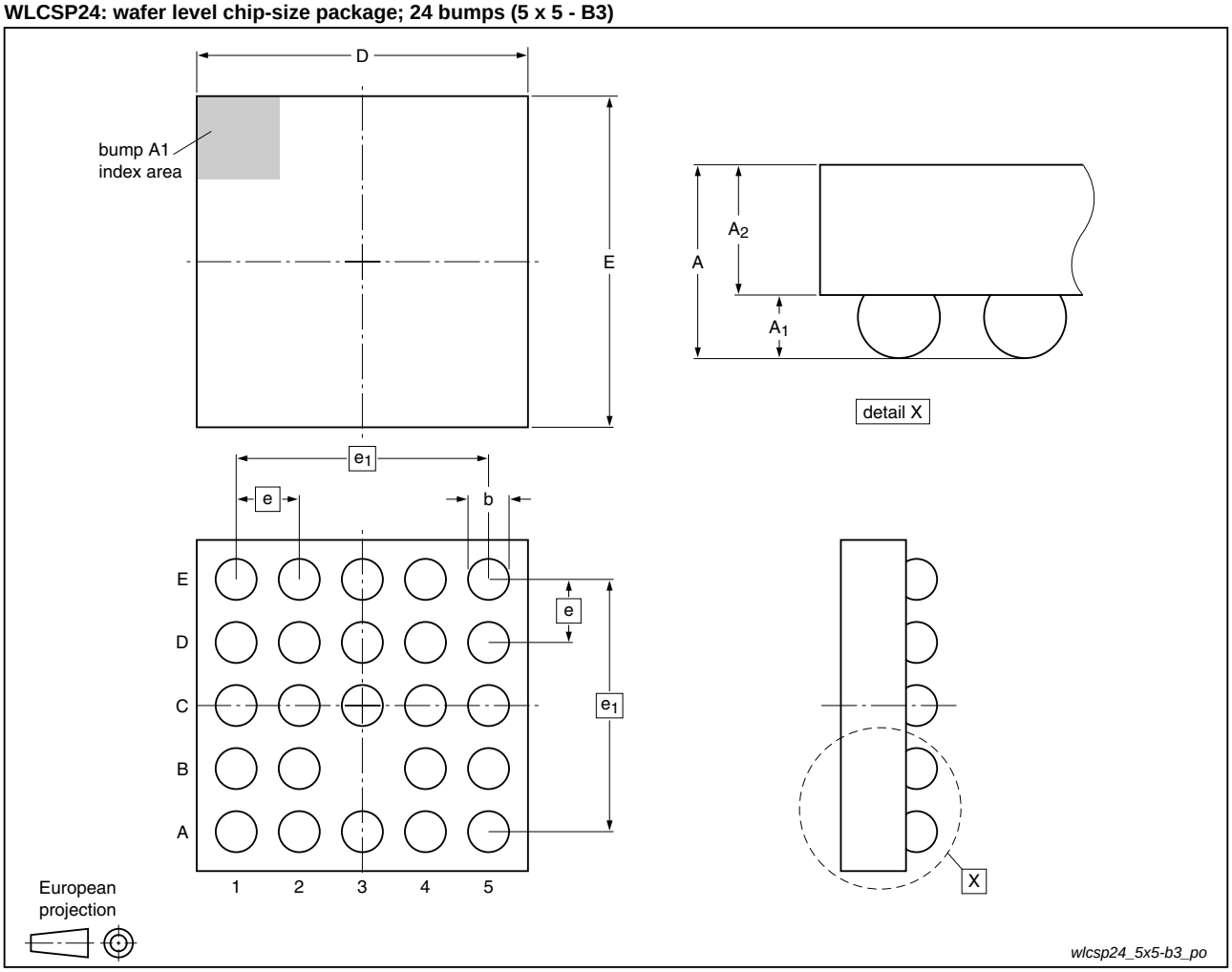


Fig 7. Package outline IP4352CX24 (WLCSP24)

Table 7. Dimensions for Figure 7

Symbol	Min	Typ	Max	Unit
A	0.56	0.61	0.66	mm
A_1	0.18	0.20	0.22	mm
A_2	0.38	0.41	0.44	mm
b	0.21	0.26	0.31	mm
D	1.96	2.01	2.06	mm
E	1.97	2.02	2.07	mm
e	0.35	0.40	0.45	mm
e_1	-	1.6	-	mm

9. Design and assembly recommendations

9.1 PCB design guidelines

For optimum performance it is recommended to use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 8 for the recommended PCB design parameters.

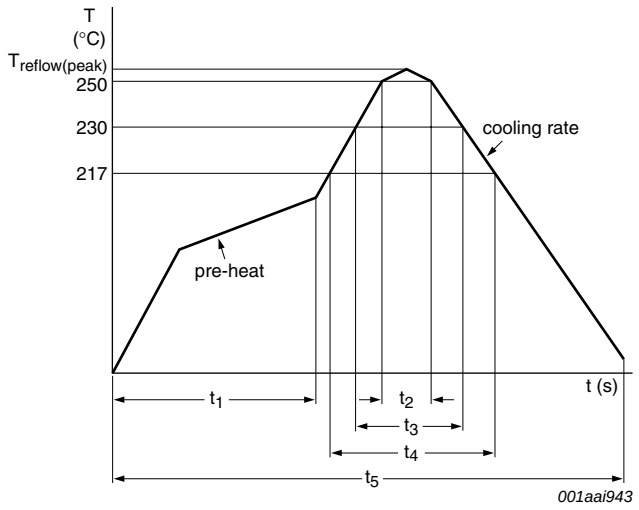
Table 8. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	200 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	370 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

9.2 PCB assembly guidelines for Pb-free soldering

Table 9. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	330 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 8



The device is capable of withstanding at least three reflows of this profile.

Fig 8. Pb-free solder reflow profile

Table 10. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
DECT	Digital Enhanced Cordless Telecommunications
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
NSMD	Non-Solder Mask PCB Design
PCB	Printed-Circuit Board
PCS	Personal Communication System
RoHS	Restriction of Hazardous Substances
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4352CX24_2	20100503	Product data sheet	-	IP4352CX24_1
Modifications:	• Features, Applications and Legal information updated. • Figure 2: Zener diode symbol added. • Figure 7: Package outline changed. • Table 6: updated. • Section 9: Soldering information changed.			
IP4352CX24_1	20090813	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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