MAX11161

16-Bit, 250ksps, +5V SAR ADC with Internal Reference in µMAX

General Description

The MAX11161 is a 16-bit, 250ksps, SAR ADC offering excellent AC and DC performance with true unipolar input range, internal reference, and small size. The MAX11161 measures a +5V (0 to 5V) input range and can operate with a single 5V supply. The MAX11161 integrates a low drift reference with internal buffer, saving the cost and space of an external reference.

This ADC achieves 92.2dB SNR at 10kHz and -106.5dB THD. The MAX11161 guarantees 16-bit no-missing codes and ±0.8 LSB INL (typ).

The MAX11161 communicates using an SPI-compatible serial interface at 2.3V, 3V, 3.3V, or 5V logic. The serial interface can be used to daisy-chain multiple ADCs for multichannel applications and provides a busy indicator option for simplified system synchronization and timing.

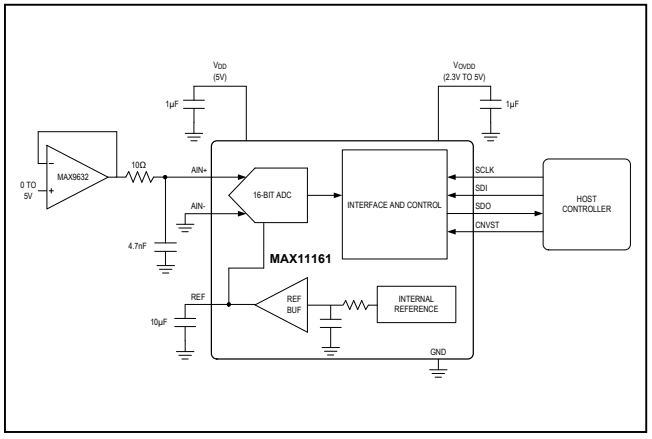
The MAX11161 is offered in a 10-pin, 3mm x 5mm, µMAX® package and is specified over the -40°C to +85°C temperature range.

Applications

- Industrial Process Control
- Data Acquisition Systems
- Medical Instrumentation
- Automatic Test Equipment

***Selector Guide* and *Ordering Information* appear at end of data sheet.**

Typical Operating Circuit



Benefits and Features

- High DC/AC Accuracy Provides Better Measurement Quality
  - 16-Bit Resolution with No Missing Codes
  - 250ksps Throughput Rates Without Pipeline Delay/Latency
  - 92.2dB SNR and -106.5dB THD at 10kHz
  - 0.5 LSB_{RMS} Transition Noise
  - ±0.8 LSB INL (typ) and ±0.3 LSB DNL (typ)
- Highly Integrated ADC Saves Cost and Space
  - ±7ppm/°C Internal Reference
  - Internal Reference Buffer
- Flexible and Low Power Supply Saves Space and Cost
  - +5V Analog and +2.3V to +5V Digital Supply
  - 31mW Power Consumption at 250ksps
  - 10µA in Shutdown Mode
- Multi-Industry Standard Serial Interface and Small Package Reduces Size
  - SPI/QSPI™/MICROWIRE®/DSP-Compatible
  - 3mm x 5mm, Tiny 10-Pin µMAX Package

14-Bit to 18-Bit SAR ADC Family

	14-BIT 500ksps	16-BIT 250ksps	16-BIT 500ksps	18-BIT 500ksps
±5V Input Internal Reference	—	MAX11167 MAX11169	MAX11166 MAX11168	MAX11156 MAX11158
0 to 5V Input Internal Reference	—	MAX11161 MAX11165	MAX11160 MAX11164	MAX11150 MAX11154
0 to 5V Input External Reference	MAX11262	MAX11163	MAX11162	MAX11152

19-7631; Rev 0; 5/15

maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
OVDD to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +6V
AIN+ to GND .....±7V
AIN-, REF,to GND.....-0.3V to the lower of (V_{DD} + 0.3V) ..... and +6V
SCLK, SDI, SDO, CNVST to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +6V
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
µMAX (derate 8.8mW/°C above +70°C) 707mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

µMAX
Junction-to-Ambient Thermal Resistance (θ_{JA}).....113°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....36°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 250ksps; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT (Note 3)						
Input Voltage Range		AIN+ to AIN-, k = 5/4.096	0		$+V_{REF}$ x k	V
Absolute Input Voltage Range		AIN+ to GND	-0.1		+5.1	V
		AIN- to GND	-0.1		+0.1	
Input Leakage Current		Acquisition phase	-10	+0.001	+10	µA
Input Capacitance				32		pF
Input-Clamp Protection Current		Both inputs	-20		+20	mA
STATIC PERFORMANCE (Note 4)						
Resolution	N		16			Bits
No Missing Codes			16			Bits
Offset Error		V_{OVDD} ≤ 3.6V	-3.5	±0.9	+3.5	LSB
		V_{OVDD} > 3.6V	-5.0		+5.0	
Offset Temperature Coefficient				±0.002		LSB/°C
Gain Error		V_{OVDD} ≤ 3.6V	-5.0		+5.0	LSB
		V_{OVDD} > 3.6V	-5.0		+5.0	
Gain Error Temperature Coefficient				±0.003		LSB/°C
Integral Nonlinearity	INL	V_{OVDD} ≤ 3.6V	-1.45	±0.8	+1.45	LSB
		V_{OVDD} > 3.6V	-1.65		+1.65	
Differential Nonlinearity	DNL	Guaranteed by design	-1.0	±0.3	+1	LSB

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 250ksps; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Full-Scale Error		V_{OVDD} ≤ 3.6V	-6.5	±2.9	+6.5	LSB
		V_{OVDD} > 3.6V	-8		+8	
Analog Input CMR	CMR	Referred to the output		-2.1		LSB/V
Power-Supply Rejection (Note 5)	PSR	PSR vs. V_{DD}, referred to the output		-5.8		LSB/V
Transition Noise				0.5		LSB_{RMS}
REFERENCE						
REF Initial Accuracy	V_{REF}		4.092	4.096	4.100	V
REF Temperature Coefficient	TC_{REF}		-17	±7	+17	ppm/°C
REF Output Impedance	Z_{REF}			0.1		Ω
DYNAMIC PERFORMANCE (Note 6)						
Signal-to-Noise Ratio	SNR		91.0	92.2		dB
Signal-to-Noise Plus Distortion	SINAD		90.7	92.0		dB
Spurious-Free Dynamic Range	SFDR	V_{OVDD} ≤ 3.6V	103.0	108.9		dB
		V_{OVDD} > 3.6V	101.0			
Total Harmonic Distortion	THD	V_{OVDD} ≤ 3.6V		-106.5	-100.4	dB
		V_{OVDD} > 3.6V			-98.0	
Intermodulation Distortion (Note 7)	IMD			-117.4		dBFS
SAMPLING DYNAMICS						
Throughput Sample Rate			0		250	ksps
Transient Response		Full-scale step			400	ns
Full-Power Bandwidth		-3dB point		6		MHz
		-0.1dB point		> 0.2		
Aperture Delay				2.5		ns
Aperture Jitter				50		ps_{RMS}
POWER SUPPLIES						
Analog Supply Voltage	V_{DD}		4.75		5.25	V
Interface Supply Voltage	V_{OVDD}		2.3		5.25	V
Analog Supply Current	I_{VDD}		4.5	5.4	6.5	mA
V_{DD} Shutdown Current				0.1	10	µA
Interface Supply Current	I_{OVDD}	V_{OVDD} = 2.3V		0.8	1.0	mA
		V_{OVDD} = 5.25V		2.1	2.7	
OVDD Shutdown Current					10	µA
Power Dissipation		V_{DD} = 5V, V_{OVDD} = 3.3V		31.0		mW

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 250ksps; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDI, SCLK, CNVST)						
Input Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{OVDD}	V
Input Hysteresis	V_{HYS}			±0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{OVDD}	-10		+10	µA
DIGITAL OUTPUT (SDO)						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				15		pF
TIMING (Note 8)						
Time Between Conversions	t_{CYC}		4			µs
Conversion Time	t_{CONV}	CNVST rising to data available	2.7		3.0	µs
Acquisition Time	t_{ACQ}	t_{ACQ} = t_{CYC} - t_{CONV}	1.0			µs
CNVST Pulse Width	t_{CNVPW}	$\overline{CS}$ mode	5			ns
SCLK Period ($\overline{CS}$ Mode)	t_{SCLK}	V_{OVDD} > 4.5V	14			ns
		V_{OVDD} > 2.7V	20			
		V_{OVDD} > 2.3V	25			
SCLK Period (Daisy-Chain Mode)	t_{SCLK}	V_{OVDD} > 4.5V	16			ns
		V_{OVDD} > 2.7V	24			
		V_{OVDD} > 2.3V	30			
SCLK Low Time	t_{SCLKL}		6			ns
SCLK High Time	t_{SCLKH}		6			ns
SCLK Falling Edge to Data Valid Delay	t_{DSDO}	V_{OVDD} > 4.5V			12	ns
		V_{OVDD} > 2.7V			18	
		V_{OVDD} > 2.3V			23	

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 250ksps; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

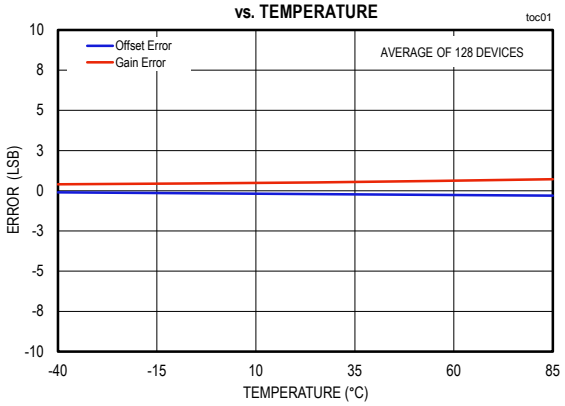
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CNVST Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}	V_{OVDD} > 2.7V			14	ns
		V_{OVDD} < 2.7V			18	
CNVST High or SDI High or Last SCLK Falling Edge to SDO High Impedance	t_{DIS}	$\overline{CS}$ mode			20	ns
SDI Valid Setup Time from CNVST Rising Edge	$t_{SSDICNV}$	4-wire $\overline{CS}$ mode	5			ns
SDI Valid Hold Time from CNVST Rising Edge	$t_{HSDICNV}$	4-wire $\overline{CS}$ mode	0			ns
SCLK Valid Setup Time from CNVST Rising Edge	$t_{SSCKCNV}$	Daisy-chain mode	3			ns
SCLK Valid Hold Time from CNVST Rising Edge	$t_{HSCKCNV}$	Daisy-chain mode	3			ns
SDI Valid Setup Time from SCLK Falling Edge	$t_{SSDISCK}$	V_{OVDD} > 4.5V, daisy-chain mode	3			ns
		V_{OVDD} > 2.7V, daisy-chain mode	5			
		V_{OVDD} > 2.3V, daisy-chain mode	6			
SDI Valid Hold Time from SCLK Falling Edge	$t_{HSDISCK}$	Daisy-chain mode	0			ns
SDI High to SDO High	$t_{DSDOSDI}$	Daisy-chain mode with busy indicator, V_{OVDD} > 4.5V			10	ns
		Daisy-chain mode with busy indicator, V_{OVDD} > 2.7V			15	
		Daisy-chain mode with busy indicator, V_{OVDD} > 2.3V			20	

Note 2: Maximum and minimum limits are fully production tested over specified supply voltage range and at a temperature of +25°C. Limits over the operating temperature range are guaranteed by design and device characterization.
Note 3: See the *Analog Inputs* and *Overvoltage Input Clamps* sections.
Note 4: Static Performance limits are guaranteed by design and device characterization. For definitions, see the *Definitions* section.
Note 5: Defined as the change in positive full-scale code transition caused by a ±5% variation in the V_{DD} supply voltage.
Note 6: 10kHz sine wave input, -0.1dB below full scale.
Note 7: f_{IN1} ~ 9.4kHz, f_{IN2} ~ 10.7kHz, Each tone at -6.1dB below full scale.
Note 8: C_{LOAD} = 65pF on SDO.

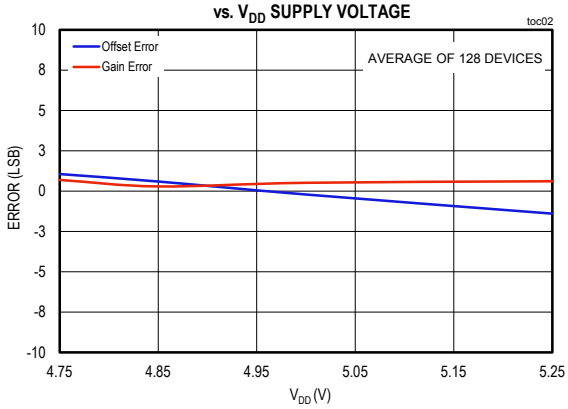
Typical Operating Characteristics

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 250ksps; T_A = +25°C, unless otherwise noted.)

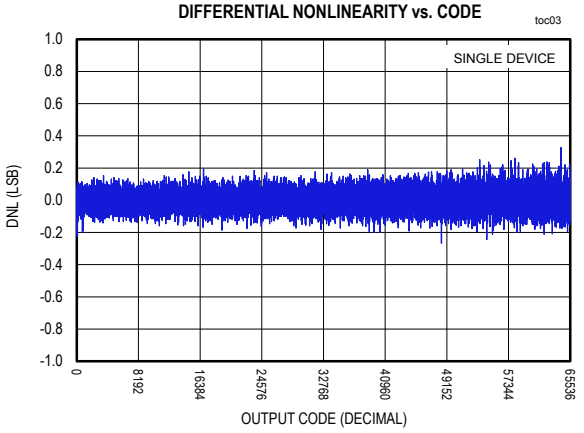
OFFSET AND GAIN ERROR vs. TEMPERATURE



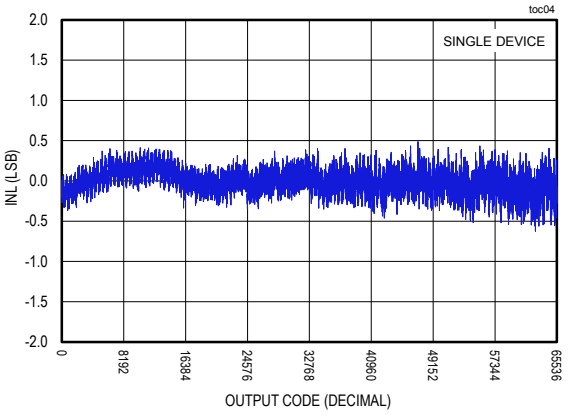
OFFSET AND GAIN ERROR vs. V_{DD} SUPPLY VOLTAGE



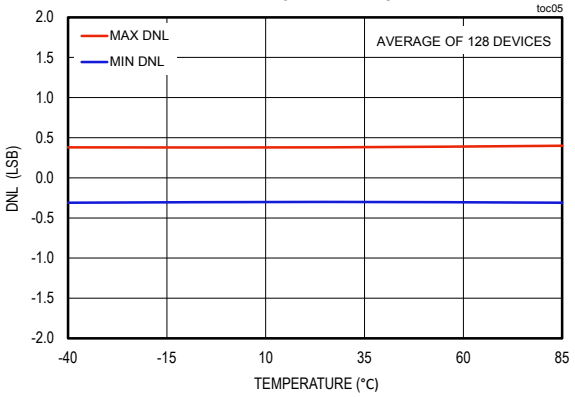
DIFFERENTIAL NONLINEARITY vs. CODE



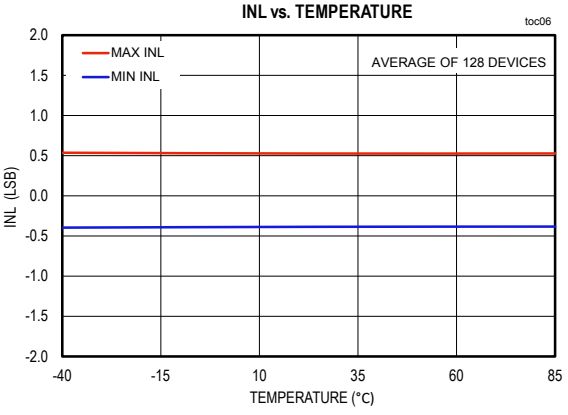
INTEGRAL NONLINEARITY vs. CODE



DNL vs. TEMPERATURE

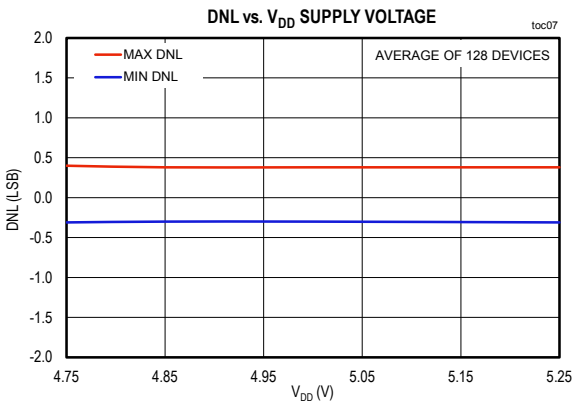


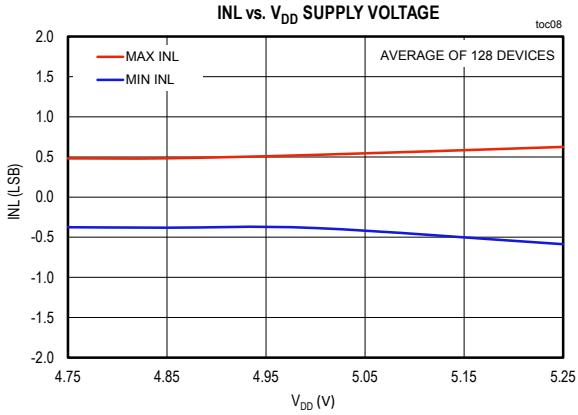
INL vs. TEMPERATURE

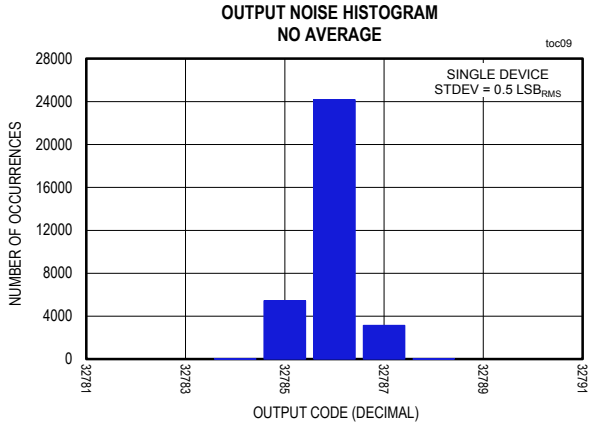


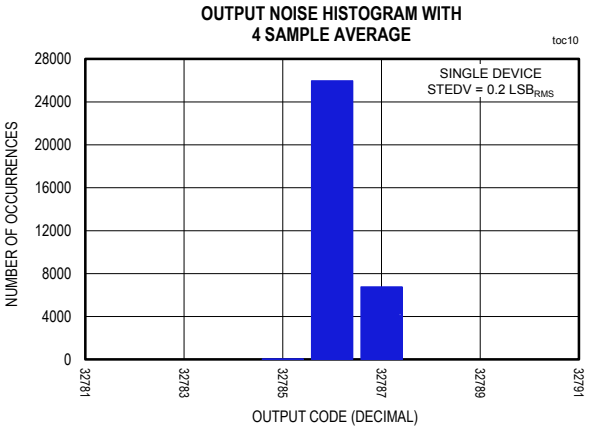
Typical Operating Characteristics (continued)

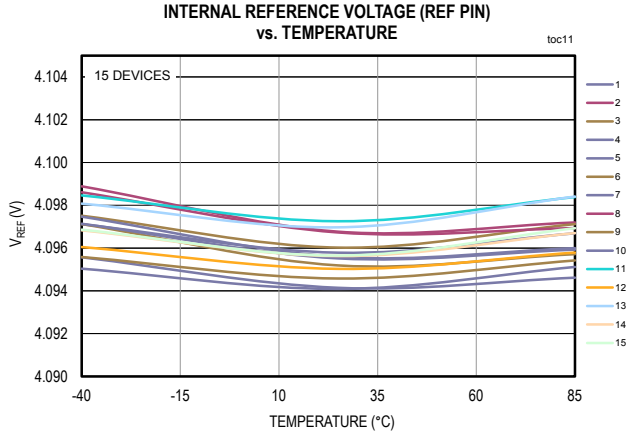
(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 250ksps; T_A = +25°C, unless otherwise noted.)

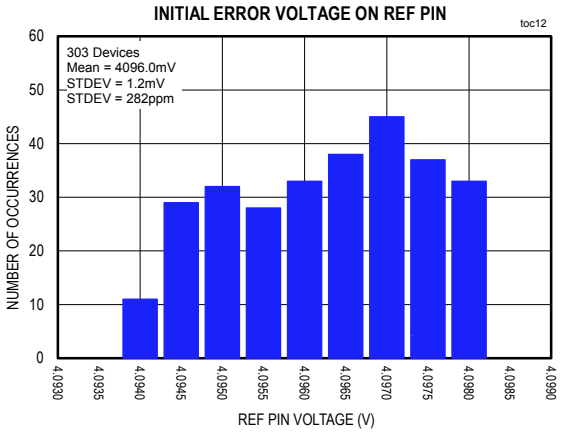








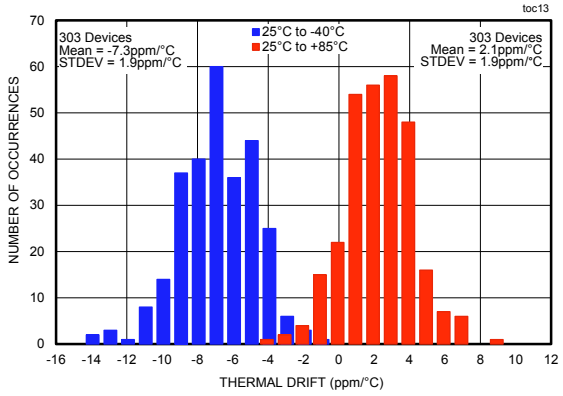




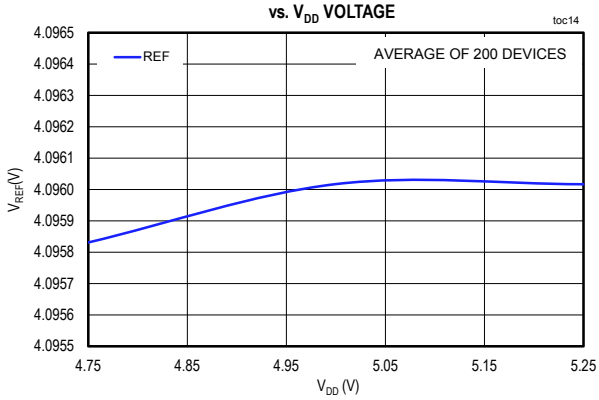
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 250ksps; T_A = +25°C, unless otherwise noted.)

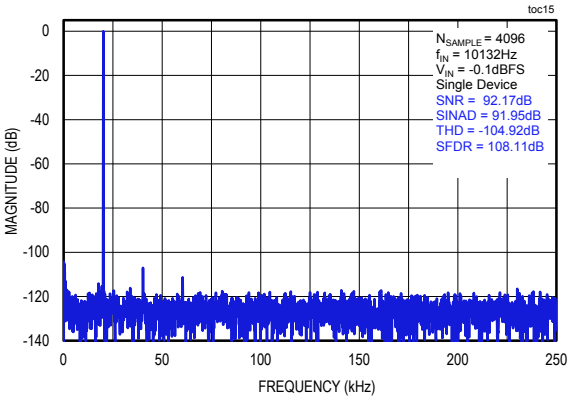
REF PIN THERMAL DRIFT SLOPE



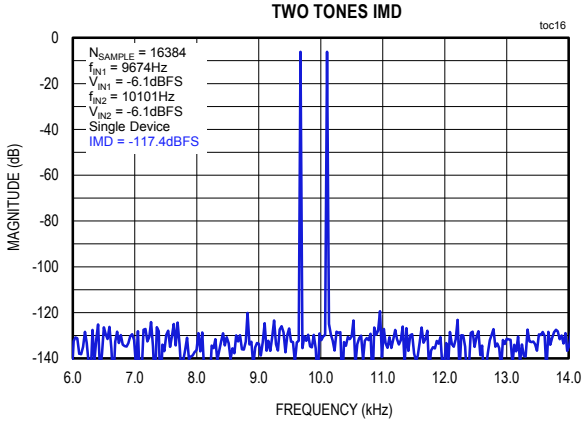
INTERNAL REFERENCE VOLTAGES vs. V_{DD} VOLTAGE



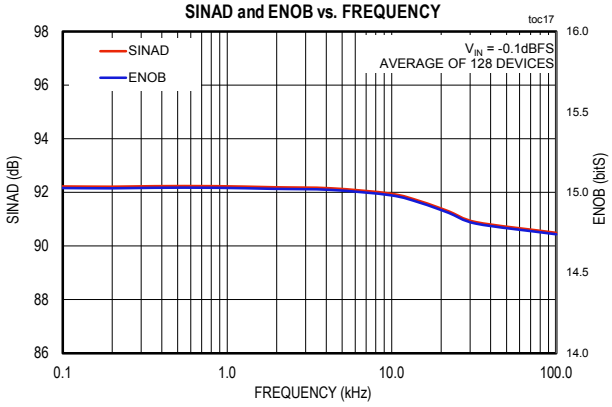
FFT PLOT



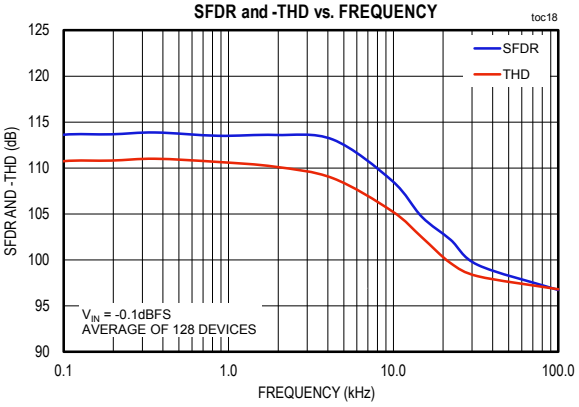
TWO TONES IMD



SINAD and ENOB vs. FREQUENCY



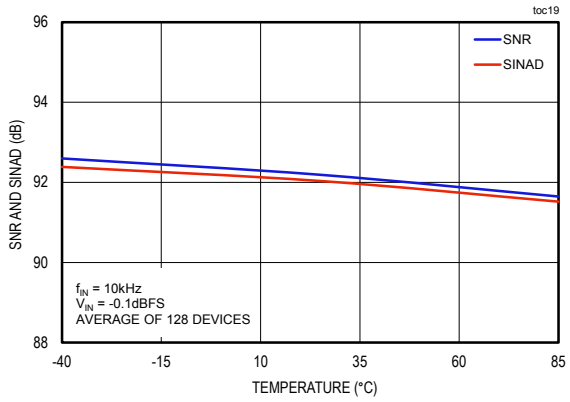
SFDR and -THD vs. FREQUENCY



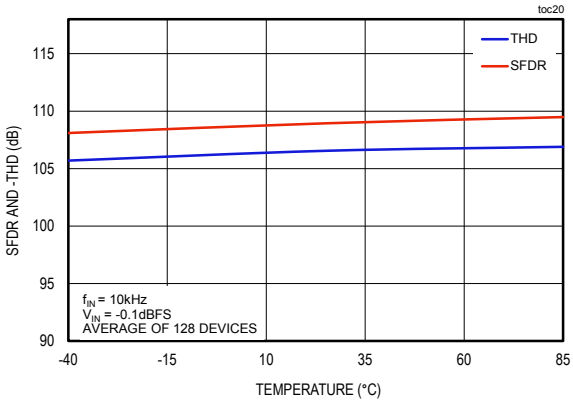
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 250ksps; T_A = +25°C, unless otherwise noted.)

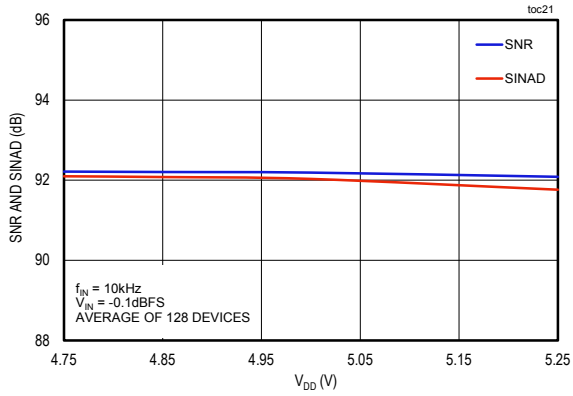
SNR and SINAD vs. TEMPERATURE



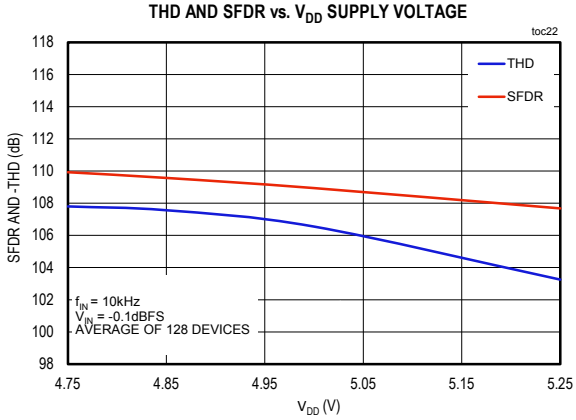
SFDR and THD vs. TEMPERATURE



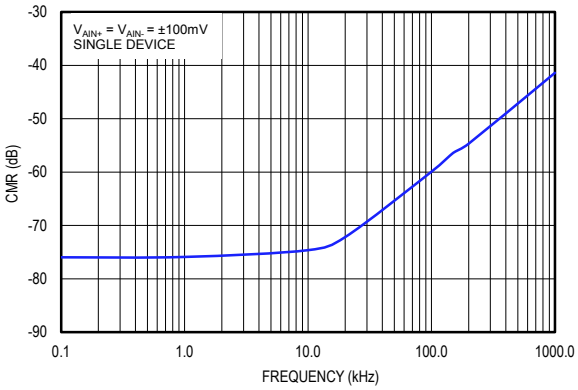
SNR and SINAD vs. V_{DD} SUPPLY VOLTAGE



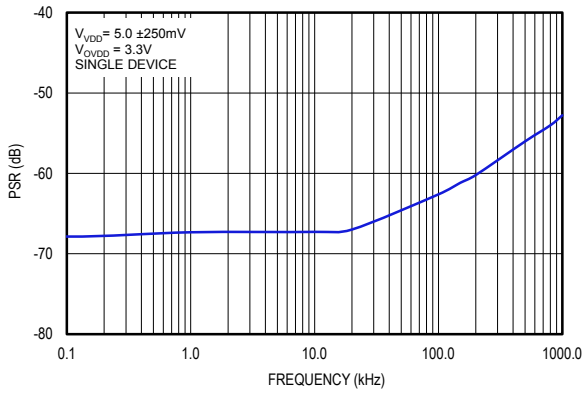
THD AND SFDR vs. V_{DD} SUPPLY VOLTAGE



CMR vs. INPUT FREQUENCY



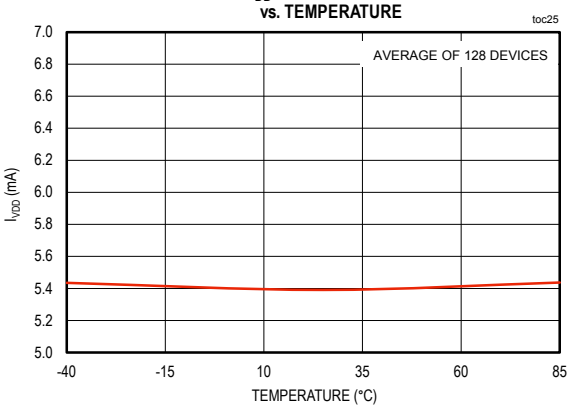
PSR vs. V_{DD} SUPPLY FREQUENCY



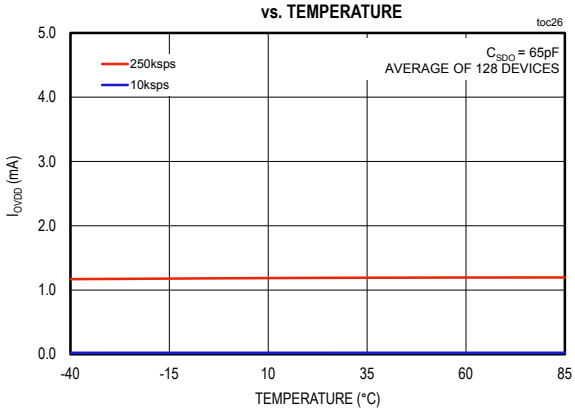
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 250ksps; T_A = +25°C, unless otherwise noted.)

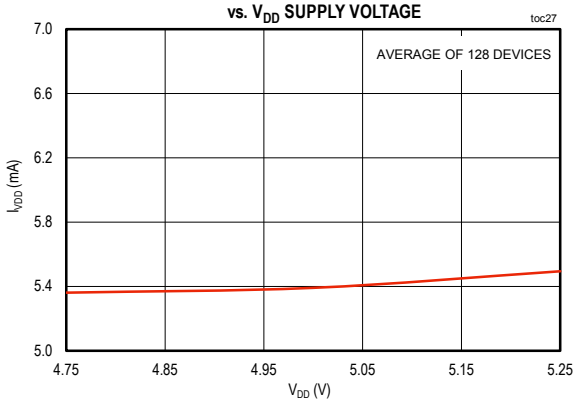
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



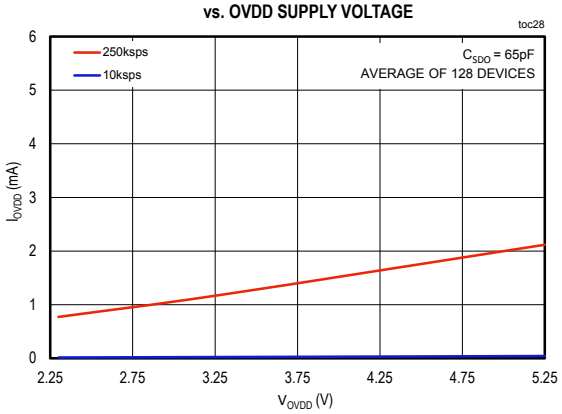
OVDD SUPPLY CURRENT vs. TEMPERATURE



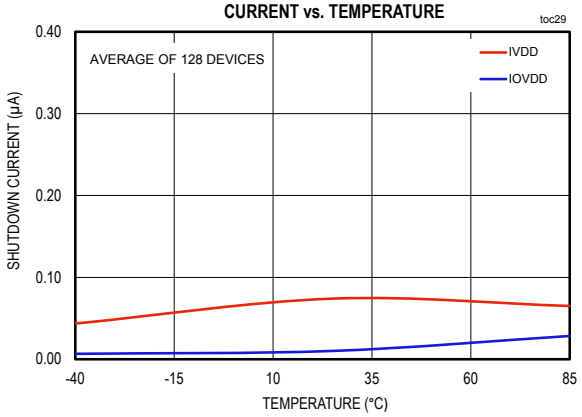
V_{DD} SUPPLY CURRENT vs. V_{DD} SUPPLY VOLTAGE



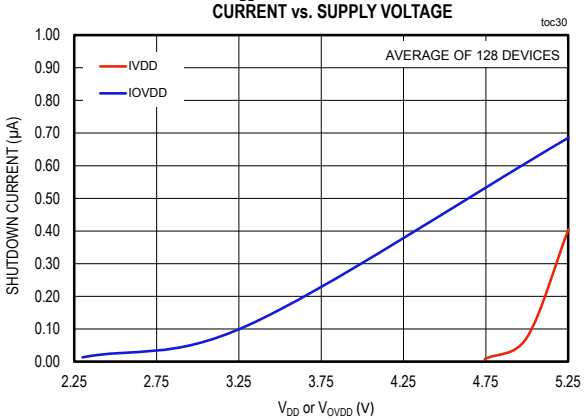
OVDD SUPPLY CURRENT vs. OVDD SUPPLY VOLTAGE



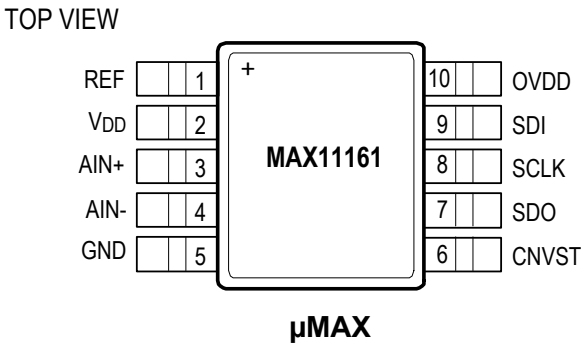
V_{DD} AND OVDD SHUTDOWN CURRENT vs. TEMPERATURE



V_{DD} AND OVDD SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



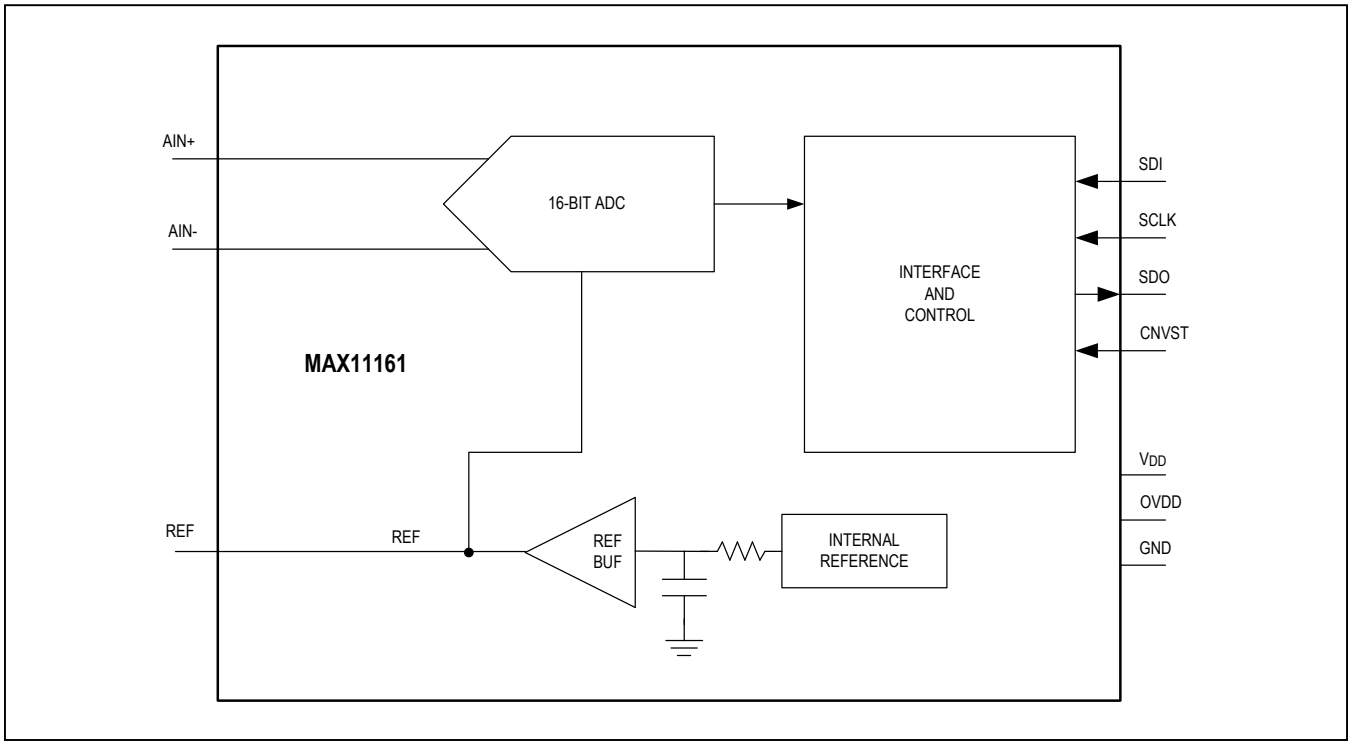
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	REF	Internal Reference Bypass. Bypass to GND in close proximity with a X5R or X7R 10µF 16V capacitor. See the *Layout, Grounding, and Bypassing* section.
2	V_{DD}	Analog Power Supply. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to each device and one 10µF capacitor per board.
3	AIN+	Positive Analog Input
4	AIN-	Negative Analog Input. Connect AIN- to the analog ground plane or to a remote sense ground.
5	GND	Power-Supply Ground
6	CNVST	Conversion Start Input. The rising edge of CNVST initiates the conversions and selects the interface mode: daisy-chain or $\overline{CS}$. In $\overline{CS}$ mode, either SDI or CNVST can enable the serial output signals when low. If SDI or CNVST is low when the conversion is completed, the busy indicator feature is enabled..
7	SDO	Serial Data Output. SDO transitions on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Clocks data out of the serial interface when the device is selected.
9	SDI	Serial Data Input and Mode Select Input. Daisy-chain mode is selected if SDI is low during the CNVST rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. $\overline{CS}$ mode is selected if SDI is high during the CNVST rising edge. In this mode, either SDI or CNVST can enable the serial output signals when low. If SDI or CNVST is low when the conversion is completed, the busy indicator feature is enabled.
10	OVDD	Digital Power Supply. OVDD can range from 2.3V to V_{DD}. Bypass OVDD to GND with a 0.1µF capacitor for each device and one 10µF per board.

Functional Diagram



Detailed Description

The MAX11161 is a 16-bit single-channel, pseudo-differential ADC with maximum throughput rates of 250ksps. Both inputs (AIN+ and AIN-) are sampled with a pseudo-differential on-chip track-and-hold.

This ADC includes a precision internal reference.

The MAX11161 allows for measuring an input voltage interval from 0 to 5V inputs that are protected for up to ±20mA of overrange current. This ADC is powered from a 4.75V to 5.25V analog supply (V_{DD}) and a separate 2.3V to 5.25V digital supply (OVDD). The MAX11161 requires 1µs to acquire the input sample on an internal track-and-hold and then converts the sampled signal to 16 bits of resolution using an internally clocked converter.

Analog Inputs

The MAX11161 ADC consists of a true sampling pseudo-differential input stage with high-impedance, capacitive inputs. The internal T/H circuitry features a small-signal bandwidth of about 6MHz to provide 16-bit accurate sampling in 1µs. This allows for accurate sampling of a number of scanned channels through an external multiplexer.

The MAX11161 accurately converts input signals on the AIN+ input in the interval from AIN- to (+5V + AIN-). AIN+ has a max input interval from -0.1V to +5.1V. AIN- has a max input interval from -0.1V to +0.1V. The MAX11161 performs a true differential sampling on inputs between AIN+ and AIN- with good common-mode rejection (see the *Typical Operating Circuit*). This allows for improved sampling of remote transducer inputs.

The MAX11161 includes a patented input switch architecture that allows direct sampling of high-impedance sources.

Overvoltage Input Clamps

The MAX11161 includes an input clamping circuit that activates when the input voltage at AIN+ is above (V_{DD} + 300mV) or below -300mV. The clamp circuit remains high impedance while the input signal is within the range of +(V_{DD} + 100mV) and -100mV and draws little to no current. However, when the input signal exceeds this range the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of -100mV to +(V_{DD} + 100mV).

To make use of the input clamps, connect a resistor (R_S) between the AIN+ input and the voltage source to limit the voltage at the analog input and to ensure the fault current into the devices does not exceed ±20mA. Note that the voltage at the AIN+ input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_S:

$$R_S = \frac{V_{FAULT\,MAX} - 7V}{20mA}$$

where $V_{FAULTMAX}$ is the maximum voltage that the source produces during a fault condition.

Figure 1 and Figure 2 illustrate the clamp circuit voltage current characteristics for a source impedance R_S = 1170Ω. While the input voltage is within the -300mV to (V_{DD} + 300mV) range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

Reference

The MAX11161 includes a precision internal reference source as well as an internal reference buffer circuit to drive the converter. The internal reference buffer requires a low inductance and ESR external decoupling capacitor of at least 10µF to be placed as close as possible to the reference pin.

Input Amplifier

The conversion results are accurate when the ADC acquires the input signal for an interval longer than the input signal's worst-case settling time. The ADC input sampling capacitor charges during the acquisition period. During this acquisition period, the settling of the sampled voltage is affected by the source resistance and the input sampling capacitance. Sampling error can be estimated by modeling the time constant of the total input capacitance and the driving source impedance.

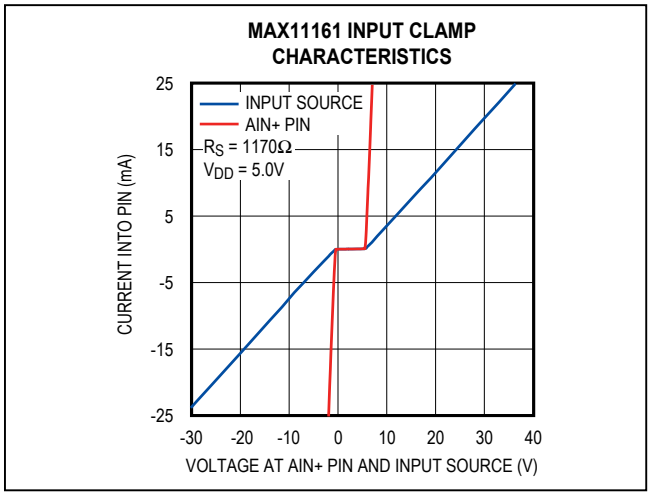


Figure 1. Input Clamp Characteristics

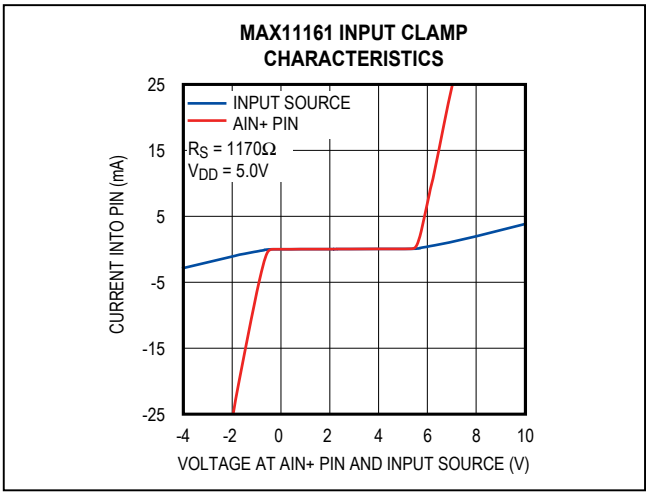


Figure 2. Input Clamp Characteristics (Zoom In)

Although the MAX11161 is easy to drive, an amplifier buffer is recommended if the source impedance is such that when driving a switch capacitor of ~32pF a settling error in the desired sampling period will occur. If this is the case, it is recommended that a configuration shown in the *Typical Operating Circuit* be used where a 4.7nF capacitor is attached to the AIN+ pin. This capacitance reduces the size of the transient at the start of the acquisition period, which will generate an input signal dependent offset error in some buffers.

Regardless of whether an external buffer amp is used or not, the time constant, $R_{SOURCE} \times C_{LOAD}$, of the input should not exceed $t_{ACQ}/12$, where R_{SOURCE} is the total signal source impedance, C_{LOAD} is the total capacitance at the ADC input (external and internal) and t_{ACQ} is the acquisition period. Thus to obtain accurate sampling in a 1µs acquisition time a source impedance of less than 1kΩ should be used if driving the ADC directly. When driving the ADC from a buffer, it is recommended a series resistance (5Ω to 50Ω typical) between the amplifier and the external input capacitance as shown in the *Typical Operating Circuit*.

These amplifier features help to select the ADC driver:

1) Fast settling time: For multichannel multiplexed applications the driving operational amplifier must be able to settle to 16-bit resolution when a full-scale step is applied during the minimum acquisition time.
2) Low noise: It is important to ensure that the driver amplifier has a low average noise density appropriate for the desired bandwidth of the application. In the case of the MAX11161, settling in a 1µs duration requires a RC filter bandwidth of approximately 4MHz. With this bandwidth, it is preferable to use an amplifier that will produce an output noise spectral density of less than 4.5nV/√Hz, to ensure that the overall SNR is not degraded significantly. It is recommended to insert an external RC filter at the MAX11161 AIN+ input to attenuate out-of-band input noise and preserve the ADCs SNR. The effective RMS noise at the MAX11161 AIN+ input is $40\mu V_{RMS}$, thus additional noise from a buffer circuit should be significantly lower to achieve the maximum SNR performance.
3) THD performance: The input buffer amplifier used should have better THD performance than the MAX11161 to ensure the THD of the digitized signal is not degraded.

Table 1 summarizes the operational amplifiers that are compatible with the MAX11161. The MAX9632 has sufficient bandwidth, low enough noise and distortion to support the full performance of the MAX11161. The MAX9633 is a dual amp and can support buffering for true pseudo-differential sampling.

Table 1. List of Recommended ADC Driver Op Amps for MAX11161

AMPLIFIER	INPUT-NOISE DENSITY (nV/√Hz)	SMALL-SIGNAL BANDWIDTH (MHz)	SLEW RATE (V/µs)	THD (dB)	I_{CC} (mA)	COMMENTS
MAX9632	0.9	55	30	-128	3.9	Low noise, THD at 10kHz
MAX9633	3	27	18	-130	3.5/amp	Low noise, dual amp, THD at 10kHz

Transfer Function

The ideal transfer characteristic for the MAX11161 is shown in Figure 3. The precise location of various points on the transfer function are given in Table 2.

Digital Interface

The MAX11161 includes three digital inputs (CNVST, SCLK, and SDI) and a single digital output (SDO). The ADC can be configured for one of six interface modes, allowing the device to support a wide variety of application needs.

The 3-wire and 4-wire $\overline{CS}$ interface modes are compatible with SPI, QSPI, digital hosts, and DSPs. The 3-wire interface uses CNVST, SCLK, and SDO for minimal wiring complexity and is ideally suited for isolated applications. The 4-wire interface allows CNVST to be independent of output data readback (SDI) affording the highest level of individual device control. This configuration is useful for low jitter or multichannel, simultaneously sampled applications.

The 3-wire daisy-chain mode is the easiest way to configure a multichannel, simultaneous-sampling system. This system is built by cascading multiple ADCs into a shift register structure. The CNVST and SCLK inputs are common to all ADCs, while the SDO output of one device feeds the SDI input of the next device in the chain. The 3-wire interface is simply the CNVST, SCLK, and SDO of the last ADC in the chain.

The selection of $\overline{CS}$ or daisy-chain modes is controlled by the SDI logic level during the rising edge of CNVST. The $\overline{CS}$ mode is selected if SDI is high and the daisy-chain mode is selected if SDI is low. If SDI and CNVST are connected together, the daisy-chain mode is selected.

In each of the three modes described above (3-wire $\overline{CS}$ mode, 4-wire $\overline{CS}$ mode, and daisy-chain mode), the user must externally time out the maximum ADC conversion time before commencing readback. Alternatively, the MAX11161 offers a busy indicator feature on SDO in each mode to eliminate external timer circuits.

When busy indication is enabled, SDO provides a busy indicator bit to signal the end of conversion. One additional SCLK is required to flush the SDO busy indication bit prior to reading back the data. Busy indicator is enabled in $\overline{CS}$ mode if CNVST or SDI is low when the ADC conversion completes. In daisy-chain mode, the busy indicator is selected based on the state of SCLK at the rising edge of CNVST. If SCLK is high, the busy indicator is enabled; otherwise, the busy indicator is not enabled.

The following sections provide specifics for each of the six serial interface modes. Due to the possibility of performance degradation, digital activity should only occur after conversion is completed or limited to the first half of the conversion phase. Having SCLK or SDI transitions near the sampling instant can also corrupt the input sample accuracy. Therefore, keep the digital inputs quiet for approximately 25ns before and 10ns after the rising edge of CNVST. These times are denoted as $t_{SSCKCNV}$ and $t_{HSCKCNV}$ in all subsequent timing diagrams.

In all interface modes, the data on SDO is valid on both SCLK edges. However, input setup time into the receiving host will be maximized when data is clocked into that host on the falling SCLK edge. Doing so will allow for higher data transfer rates between the MAX11161 and the receiving host and consequently higher converter throughput.

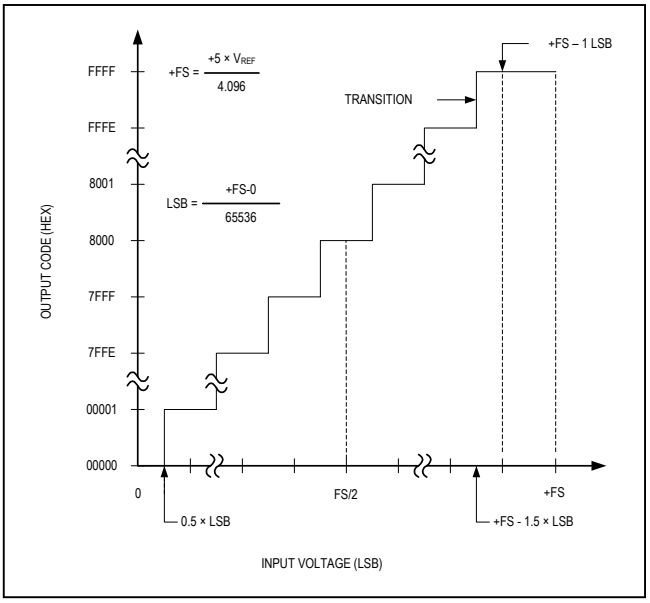


Figure 3. Unipolar Transfer Function

Table 2. Transfer Function Example

CODE TRANSITION	UNIPOLAR INPUT (V)	DIGITAL OUTPUT CODE (HEX)
+FS - 1.5 LSB	+4.999886	FFFE - FFFF
Midscale + 0.5 LSB	2.500038	8000 - 8001
Midscale	2.500000	8000
Midscale - 0.5 LSB	2.499962	7FFF - 8000
+ 0.5 LSB	0.000038	0000 - 0001

Shutdown

In all interface modes, the MAX11161 can be placed into a shutdown state by holding SCLK high while pulling CNVST from high to low. Supply current is reduced to less than 10µA on both V_{DD} and OVDD supplies (see Figure 4). To wake up from shutdown mode, hold SCLK low and pull CNVST from high to low.

ADC Modes of Operation

The MAX11161 six modes of operation are summarized in Table 3. For each of the six modes of operation a typical application model and list of benefits are described.

$\overline{CS}$ Mode 3-Wire, No-Busy Indicator

The 3-wire $\overline{CS}$ mode with no-busy indicator is ideally suited for isolated applications that require minimal wiring complexity. In Figure 5, a single ADC is connected to an SPI-compatible digital host with corresponding timing given in Figure 6.

With SDI connected to OVDD, a rising edge on CNVST completes the acquisition, initiates the conversion and forces SDO to high impedance. The conversion continues to completion irrespective of the state of CNVST, allowing CNVST to be used as a select line for other devices on the board. CNVST must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid generating the busy signal indicator.

When the conversion is complete, the MAX11161 enters the acquisition phase. Drive CNVST low to output the MSB onto SDO. The remaining data bits are then clocked by subsequent SCLK falling edges. SDO returns to high impedance after the 16th SCLK falling edge or when CNVST goes high.

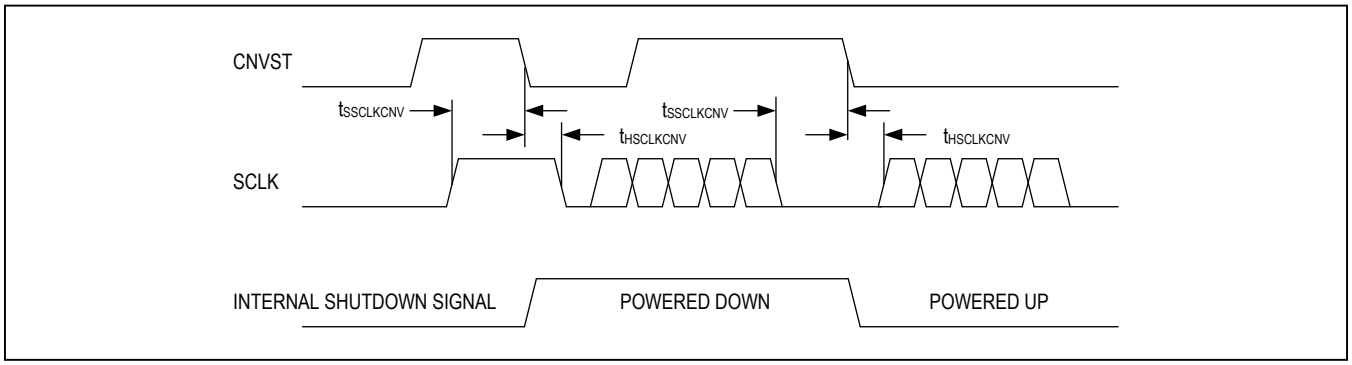


Figure 4. Entering and Exiting Shutdown Mode

Table 3. ADC Modes of Operation

MODE	TYPICAL APPLICATION AND BENEFITS
$\overline{CS}$ Mode 3-Wire, No-Busy Indicator	Single ADC connected to SPI-compatible digital host. Minimal wiring complexity; ideally suited for isolated applications.
$\overline{CS}$ Mode 3-Wire, With Busy Indicator	Single ADC connected to SPI-compatible digital host with interrupt input. Minimal wiring complexity; ideally suited for isolated applications.
$\overline{CS}$ Mode 4-Wire, No-Busy Indicator	Multiple ADCs connected to SPI-compatible digital host. CNVST used for acquisition and conversion; ideally suited for low jitter applications and simultaneous sampling. SDI used to control data readback.
$\overline{CS}$ Mode 4-Wire, With Busy Indicator	Single ADC connected to SPI-compatible digital host with interrupt input. CNVST used for acquisition and conversion; ideally suited for low jitter applications.
Daisy-Chain Mode, No-Busy Indicator	Multiple ADCs connected to 3-wire serial interface. Minimal wiring complexity; ideally suited for multichannel simultaneous sampled isolated applications.
Daisy-Chain Mode, With Busy Indicator	Multiple ADCs connected to 3-wire serial interface with busy indicator. Minimal wiring complexity; ideally suited for multichannel simultaneous sampled isolated applications.

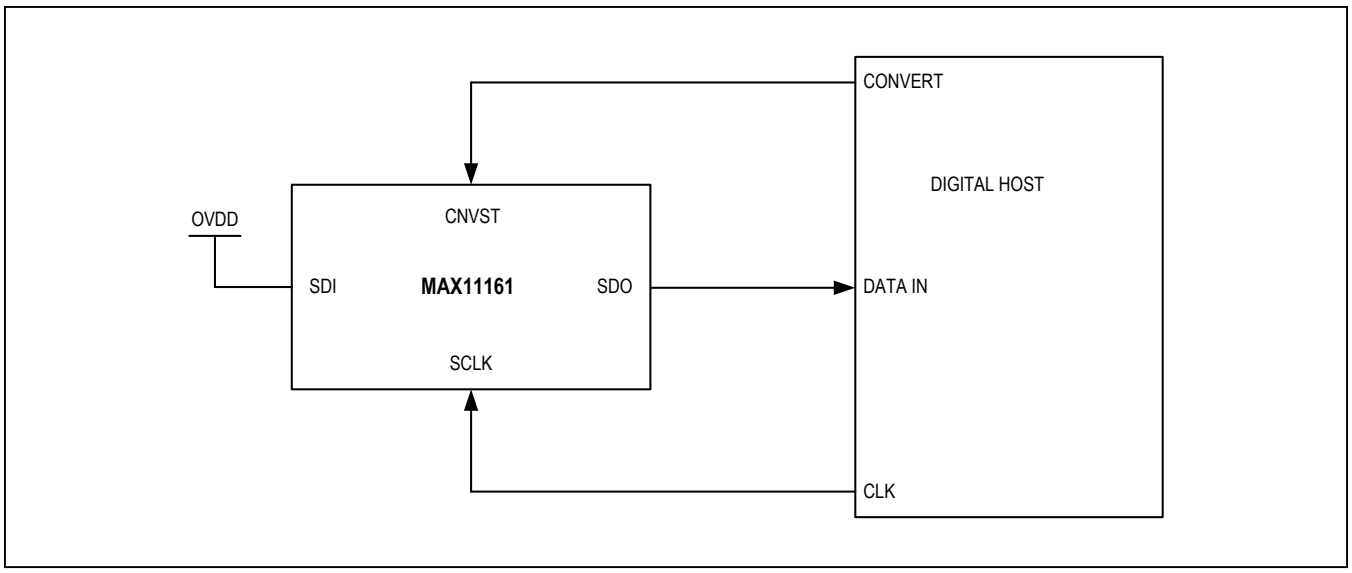


Figure 5. $\overline{CS}$ Mode 3-Wire, No-Busy Indicator Connection Diagram (SDI High)

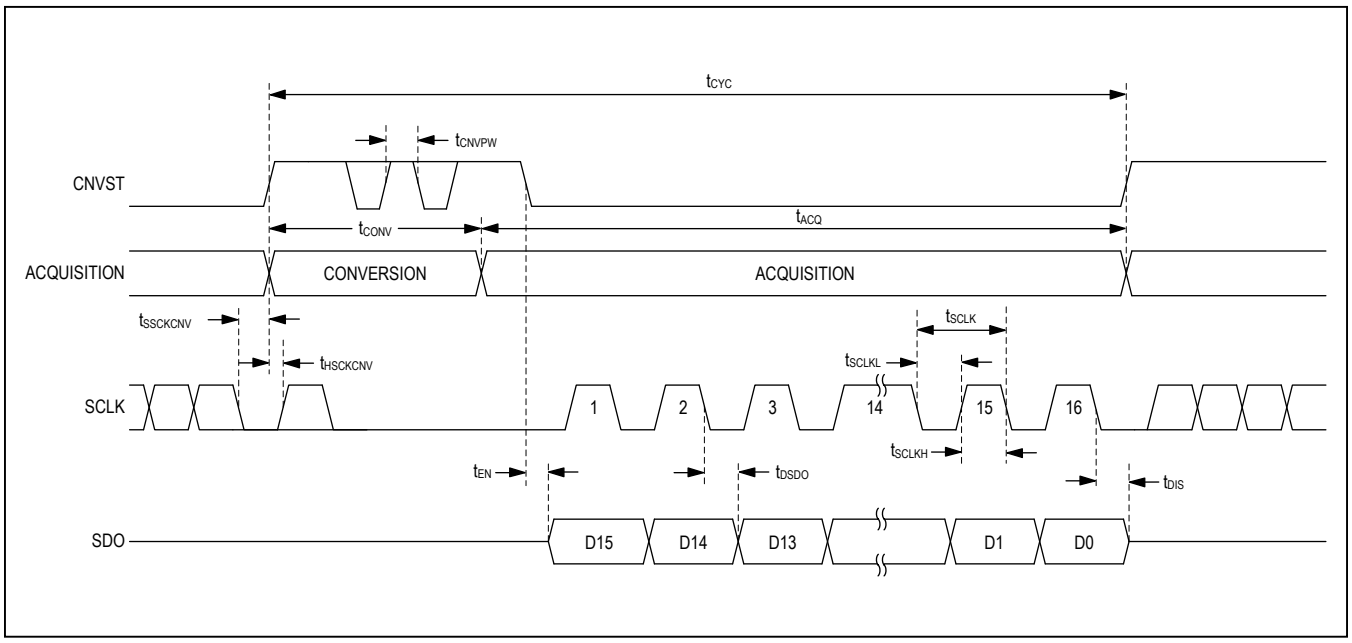


Figure 6. $\overline{CS}$ Mode 3-Wire, No-Busy Indicator Serial Interface Timing (SDI High)

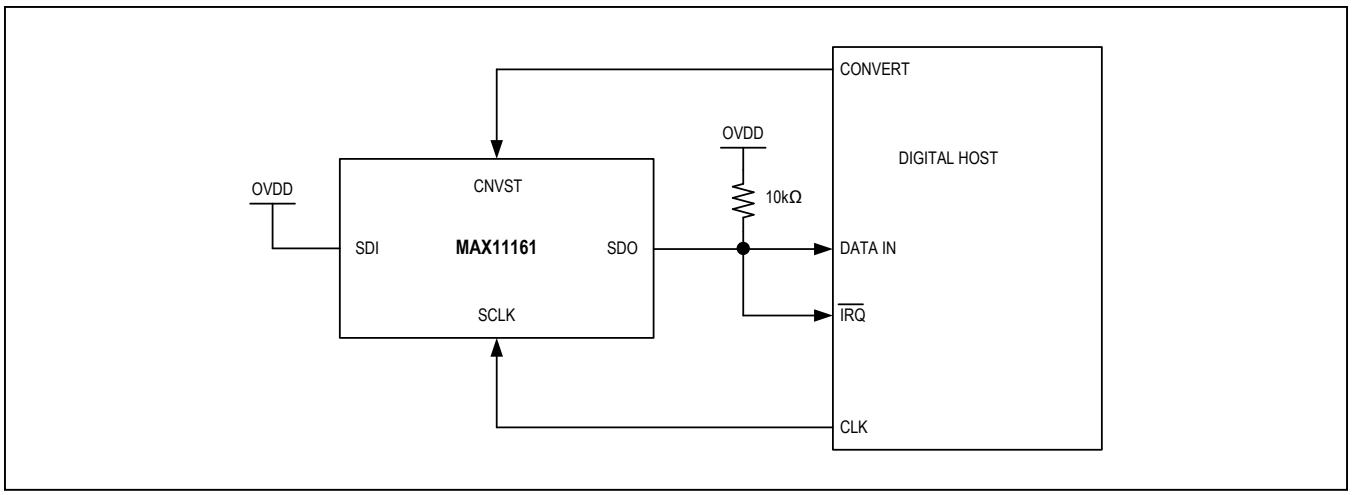


Figure 7. $\overline{CS}$ Mode 3-Wire with Busy Indicator Connection Diagram (SDI High)

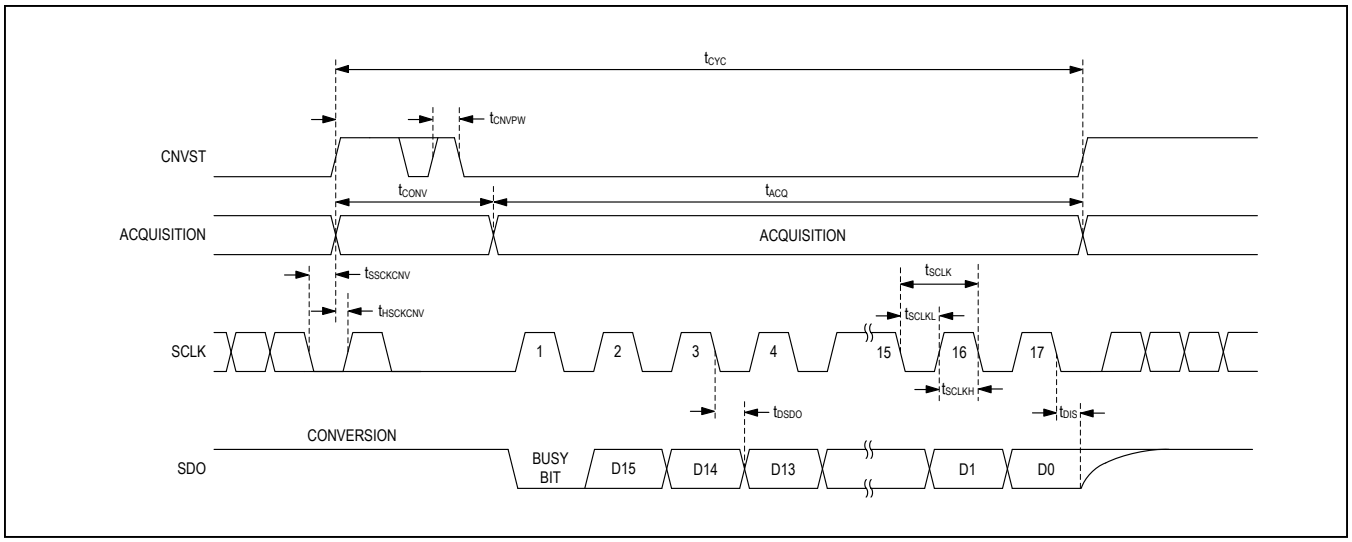


Figure 8. $\overline{CS}$ Mode 3-Wire with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 3-Wire, With Busy Indicator

The 3-wire $\overline{CS}$ mode with busy indicator is shown in Figure 7 where a single ADC is connected to an SPI-compatible digital host with interrupt input. The corresponding timing is given in Figure 8.

With SDI connected to OVDD, a rising edge on CNVST completes the acquisition, initiates the conversion and forces SDO to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board. CNVST must be returned low before the minimum conversion time and held low until the busy signal is generated. When the conversion is complete, SDO transitions from high impedance to a low logic level signaling to the digital host through the interrupt input that data readback can commence. The MAX11161 then enters the acquisition phase. The data bits are clocked out, MSB first, by subsequent SCLK falling edges. SDO returns to high impedance after the 17th SCLK falling edge or when CNVST goes high and is then pulled to OVDD through the external pullup resistor.

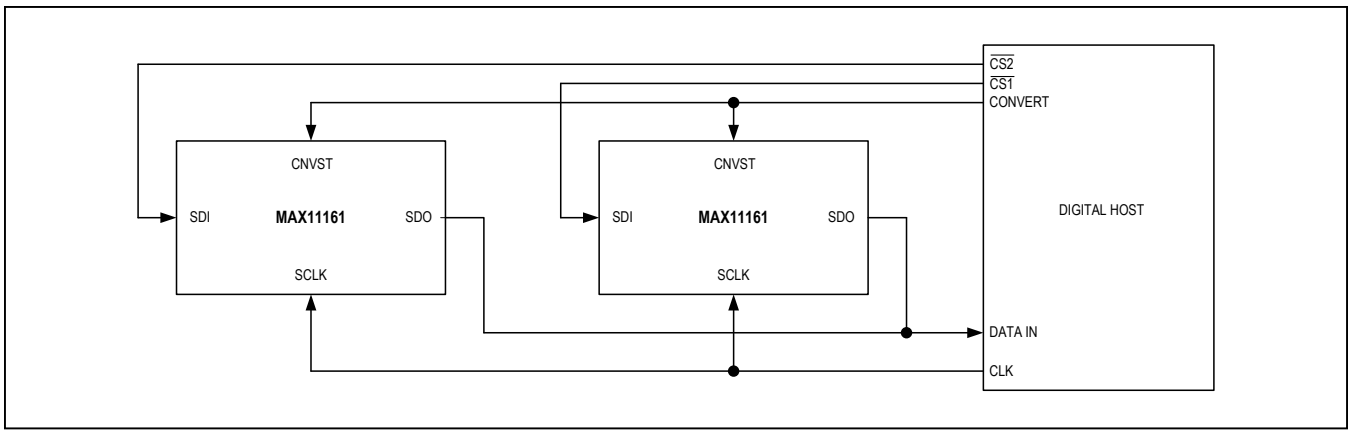


Figure 9. $\overline{CS}$ Mode 4-Wire, No-Busy Indicator Connection Diagram

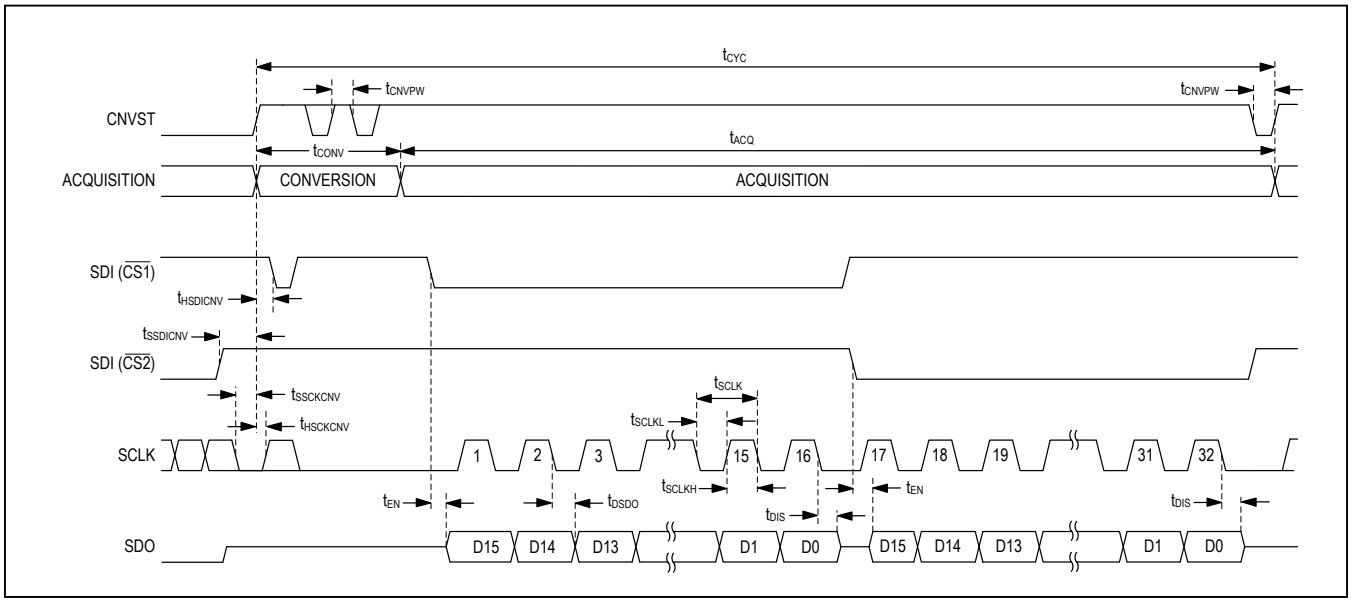


Figure 10. $\overline{CS}$ Mode 4-Wire, No-Busy Indicator Serial Interface Timing

$\overline{CS}$ Mode 4-Wire, No-Busy Indicator

The 4-wire $\overline{CS}$ mode with no-busy indicator is ideally suited for multichannel applications. In this case, the CNVST pin may be used for low-jitter simultaneous sampling while the SDI pin(s) are used to control data readback. In Figure 9, two ADCs are connected to an SPI-compatible digital host with corresponding timing given in Figure 10.

With SDI high, a rising edge on CNVST completes the acquisition, initiates the conversion, and forces SDO to high impedance. This mode requires CNVST to be held high during the conversion and data readback phases. Note that if CNVST and SDI are low, SDO is driven low.

During the conversion, the SDI pin(s) can be used as a select line for other devices on the board, but must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid generating the busy signal indicator.

When the conversion is complete, the MAX11161 enters the acquisition phase. ADC data is read by driving its respective SDI line low, outputting the MSB onto SDO. The remaining data bits are then clocked by subsequent SCLK falling edges. SDO returns to high impedance after the 16th SCLK falling edge or when CNVST goes high.

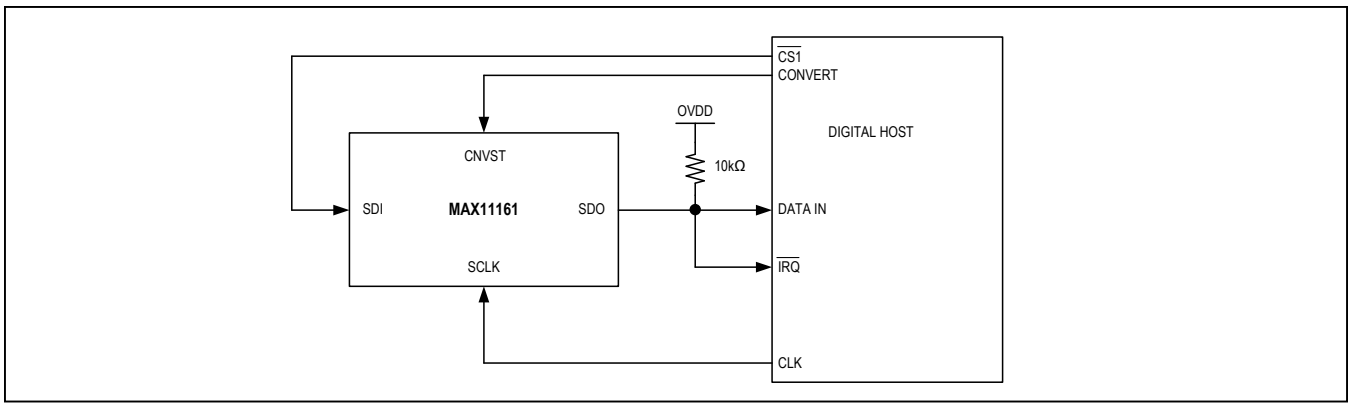


Figure 11. CS Mode 4-Wire with Busy Indicator Connection Diagram

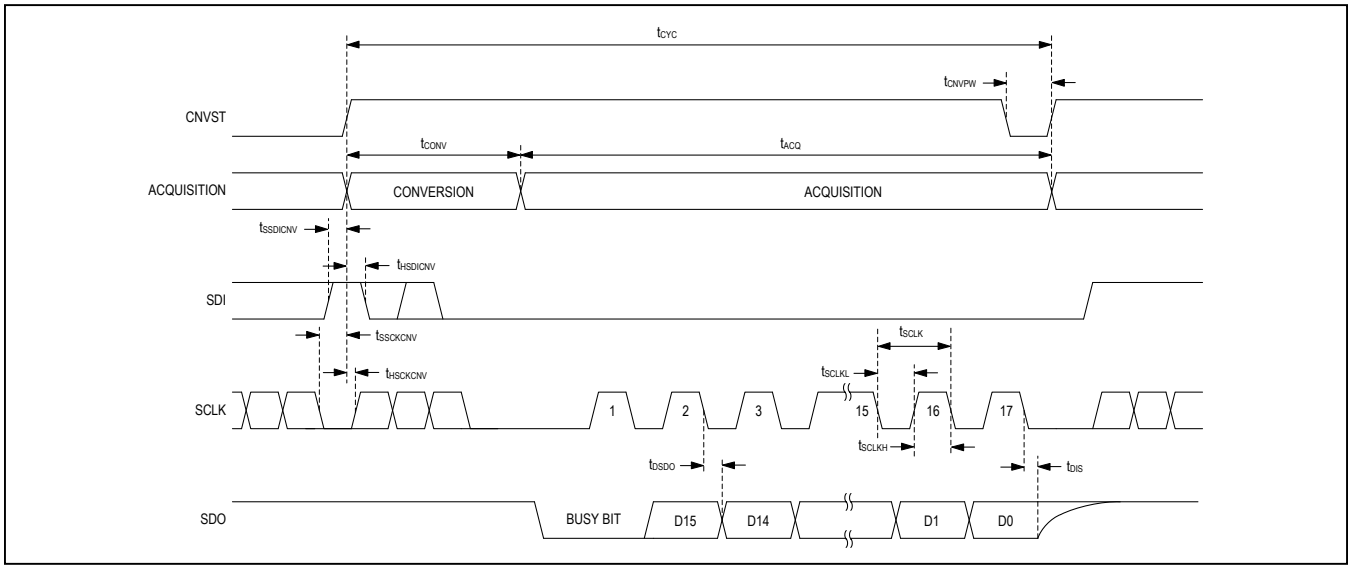


Figure 12. CS Mode 4-Wire with Busy Indicator Serial Interface Timing

CS Mode 4-Wire, With Busy Indicator

The 4-wire CS mode with busy indicator is shown in Figure 11 where a single ADC is connected to an SPI-compatible digital host with interrupt input. The corresponding timing is given in Figure 12. This mode is ideally suited for single ADC applications where the CNVST pin may be used for low-jitter sampling while the SDI pin is used for data read-back.

With SDI high, a rising edge on CNVST completes the acquisition, initiates the conversion and forces SDO to high impedance. This mode requires CNVST to be held high during the conversion and data readback phases. Note that if CNVST and SDI are low, SDO is driven low. During the conversion, the SDI pin can be used as a select line for other devices on the board, but must be returned low before the minimum conversion time and held low until the busy signal is generated.

When the conversion is complete SDO transitions from high impedance to a low logic level signaling to the digital host through the interrupt input that data readback can commence. The MAX11161 then enters the acquisition phase. The data bits are clocked out, MSB first, by subsequent SCLK falling edges. SDO returns to high impedance after the 17th SCLK falling edge or when CNVST goes high and is then pulled to OVDD through the external pullup resistor.

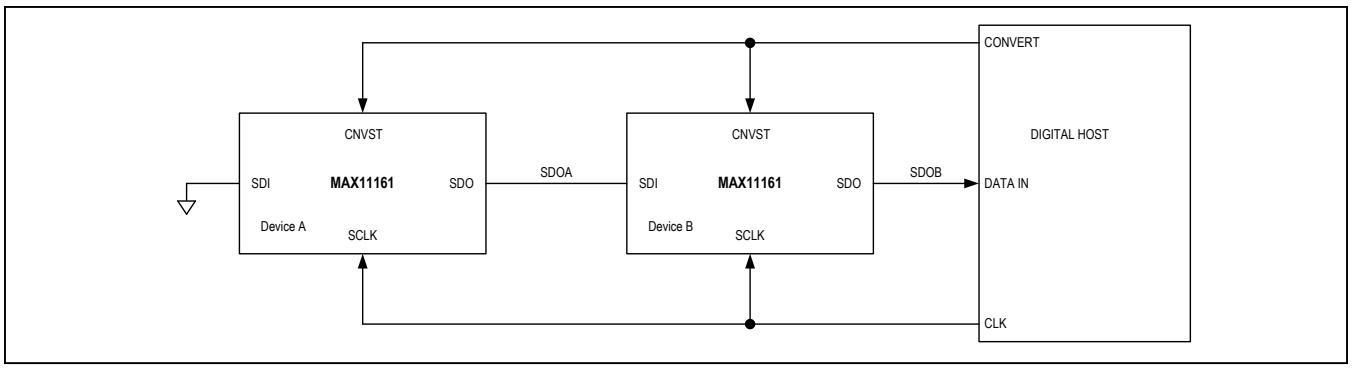


Figure 13. Daisy-Chain Mode, No-Busy Indicator Connection Diagram

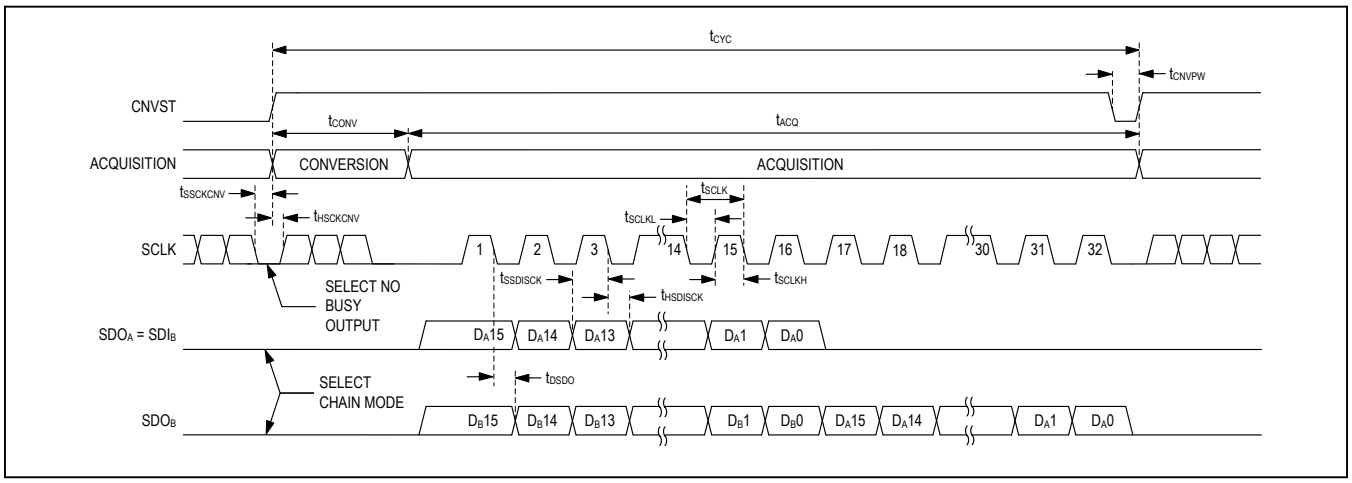


Figure 14. Daisy-Chain Mode, No-Busy Indicator Serial Interface Timing

Daisy-Chain Mode, No-Busy Indicator

The daisy-chain mode with no-busy indicator is ideally suited for multichannel isolated applications that require minimal wiring complexity. Simultaneous sampling of multiple ADC channels is realized on a 3-wire serial interface where data readback is analogous to clocking a shift register. In Figure 13, two ADCs are connected to an SPI-compatible digital host with corresponding timing given in Figure 14.

The daisy-chain mode is engaged when the MAX11161 detects the low state on SDI at the rising edge of CNVST. In this mode, CNVST is brought low and then high to trigger the completion of the acquisition phase and the start of a conversion. A low SCLK state on the rising edge of CNVST signals to the internal controller that the no-busy indicator will be output. When in chain mode, the SDO output is driven active at all times.

When SDI and CNVST are both low, SDO is driven low, thus engaging the daisy-chain mode of operations on the downstream MAX11161 parts. For example, in Figure 13 part A has its SDI tied low so the chain mode of operation will be selected on every conversion. When CNVST goes low to trigger another conversion, part A's SDO and consequently part B's SDI go low as well. On the next CNVST rising edge both parts A and B will select the daisy-chain mode interface.

When a conversion is complete, the MSB is presented onto SDO, and the MAX11161 returns to the acquisition phase. The remaining data bits, stored within the internal shift register, are clocked out on each subsequent SCLK falling edge. The SDI input of each ADC in the chain is used to transfer conversion data from the previous ADC into the internal shift register of the next ADC, thus allowing for data to be clocked through the multichip chain on each SCLK falling edge. Each ADC in the chain outputs its MSB data first requiring 16 × N clocks to read back N ADCs.

In daisy-chain mode, the maximum conversion rate is reduced due to the increased readback time. For instance, with a 6ns digital host setup time and 3V interface, up to four MAX11161 devices running at a conversion rate of 218ksps can be daisy-chained on a 3-wire port.

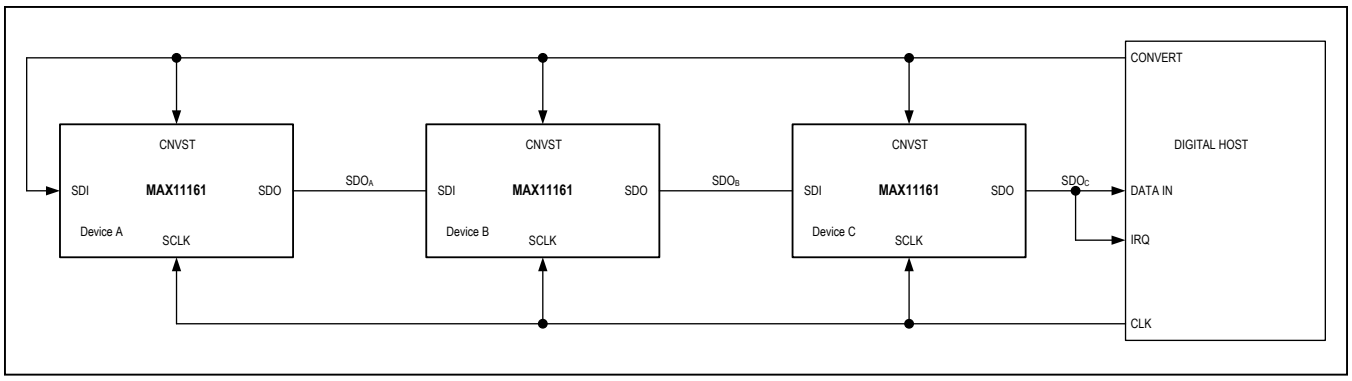


Figure 15. Daisy-Chain Mode with Busy Indicator Connection Diagram

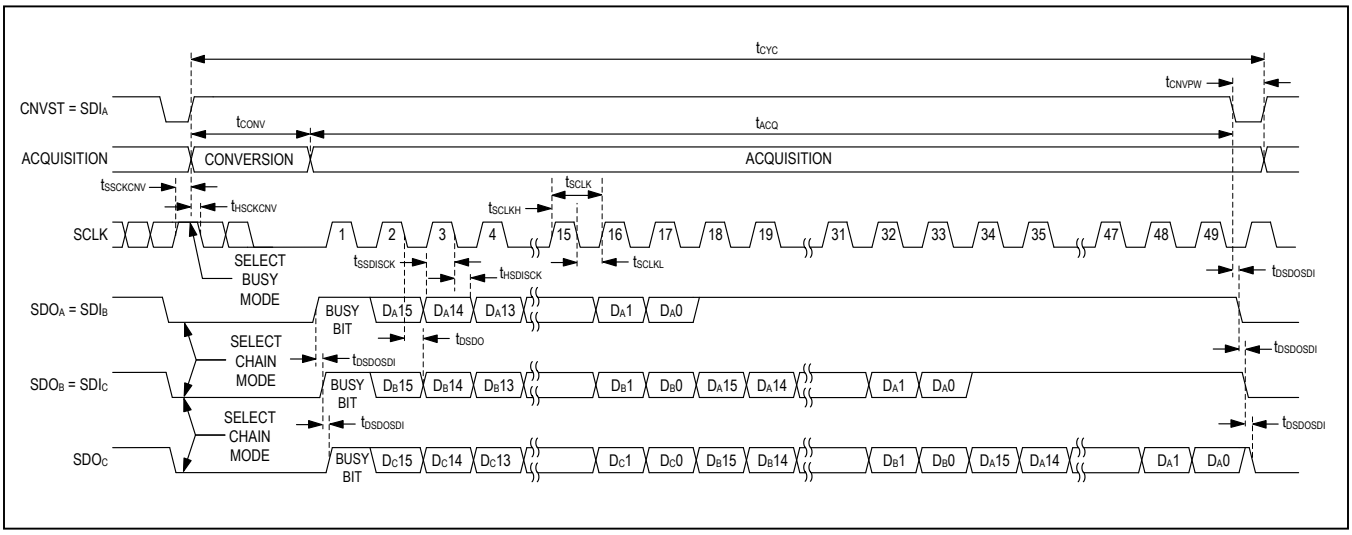


Figure 16. Daisy-Chain Mode with Busy Indicator Serial Interface Timing

Daisy-Chain Mode, With Busy Indicator

The daisy-chain mode with busy indicator is shown in Figure 15 where three ADCs are connected to an SPI-compatible digital host with corresponding timing given in Figure 16.

The daisy-chain mode is engaged when the MAX11161 detects a low state on SDI at the rising edge of CNVST. Additionally, SDI can be tied directly to CNVST to trigger the chain interface mode. In this mode, CNVST is brought low and then high to trigger the completion of the acquisition phase and the start of a conversion. A high SCLK state on the rising edge of CNVST signals to the internal controller that the busy indicator will be outputted. When in daisy-chain mode, the SDO output is driven active at all times.

When SDI and CNVST are both low, SDO is driven low, thus engaging the daisy-chain mode of operations on the downstream MAX11161 parts. For example, in Figure 15 part A has its SDI tied low so the daisy-chain mode of operation will be selected on every conversion. When CNVST goes low to trigger another conversion, part A's SDO and consequently part B's SDI go low as well. The same is true on part C's SDI input. Consequently, on the next CNVST rising edge all parts in the chain will select the daisy-chain mode interface.

When a conversion is complete, the busy indicator is presented onto each SDO, and the MAX11161 returns to the acquisition phase. As each part completes its conversion, it looks for a busy enable signal on its SDI pin from the earlier part in the chain. When it sees a busy enable signal on its input and its own conversion has completed, it enables its busy output signal on SDO. Thus the busy enable signals are propagated down the chain and the final busy enable signal at the host indicates that all devices in the chain have completed their conversion and all can be readout.

The conversion data bits are stored within the internal shift register and clocked out on each subsequent SCLK falling edge. The SDI input of each ADC in the chain is used to transfer conversion data from the previous ADC into the internal shift register of the next ADC, thus allowing for data to be clocked through the multichip chain on each SCLK falling edge. With busy indicator mode selected, the busy bit from each part is not chained on the first falling SCLK edge in the readout pattern. Consequently, the number of falling SCLKs needed to read back all data from N ADCs is 16 × N + 1 falling edges.

In daisy-chain mode, the maximum conversion rate is reduced due to the increased readback time. For instance, with a 6ns digital host setup time and 3V interface, up to four MAX11161 devices running at a conversion rate of 217ksps can be daisy-chained on a 3-wire port.

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect the GND pin on the MAX11161 to this ground plane. Keep the ground return to the power supply low impedance and as short as possible for noise-free operation.

A 4.7nF C0G (or NPO) ceramic chip capacitor should be placed between AIN+ and the ground plane as close as possible to the MAX11161. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit. If AIN- is to be used for remote sense, put a matching 4.7nF C0G ceramic capacitor as close to this pin as well to minimize the effect to the inductance in the remote sense line.

For best performance, decouple the REF output to the ground plane with a 16V, 10µF or larger ceramic chip capacitor with a X5R or X7R dielectric in a 1210 or smaller case size. Ensure that all bypass capacitors are connected directly into the ground plane with an independent via.

Bypass V_{DD} and OVDD to the ground plane with 0.1µF ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10µF decoupling capacitor to V_{DD} and OVDD per PCB. For best performance, bring a V_{DD} power plane in on the analog interface side of the MAX11161 and a OVDD power plane from the digital interface side of the device.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

For the MAX11161, the offset error is defined at code center 0x0000. This code center should occur at 0V input between AIN+ and AIN-. The offset error is the actual voltage required to produce code center 0x0000, expressed in LSB.

Gain Error

Gain error is defined as the difference between the actual change in analog input voltage required to produce a top code transition minus a bottom code transition, and the ideal change in analog input voltage range to produce the same code transitions. It is expressed in LSB.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input power to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the power signal to the power noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's power to the power of all the other ADC output signals:

$$SINAD(dB) = 20 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits

The effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the power contained in the first five harmonics of the converted data to the power of the fundamental. This is expressed as:

$$THD = 10 \times \log\left[\frac{P_2 + P_3 + P_4 + P_5}{P_1}\right]$$

where P_1 is the fundamental power and P_2 through P_5 is the power of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the power of the fundamental (maximum signal component) to the power of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Selector Guide

PART	BITS	INPUT RANGE (V)	REFERENCE	PACKAGE	SPEED (ksps)
MAX11262	14	0 to 5	External	3mm x 5mm µMAX-10	500
MAX11160	16	0 to 5	Internal	3mm x 5mm µMAX-10	500
MAX11161	16	0 to 5	Internal	3mm x 5mm µMAX-10	250
MAX11162	16	0 to 5	External	3mm x 5mm µMAX-10	500
MAX11163	16	0 to 5	External	3mm x 5mm µMAX-10	250
MAX11164	16	0 to 5	Internal/External	3mm x 3mm TDFN-12	500
MAX11165	16	0 to 5	Internal/External	3mm x 3mm TDFN-12	250
MAX11166	16	±5	Internal/External	3mm x 3mm TDFN-12	500
MAX11167	16	±5	Internal/External	3mm x 3mm TDFN-12	250
MAX11168	16	±5	Internal	3mm x 5mm µMAX-10	500
MAX11169	16	±5	Internal	3mm x 5mm µMAX-10	250
MAX11150	18	0 to 5	Internal	3mm x 5mm µMAX-10	500
MAX11152	18	0 to 5	External	3mm x 5mm µMAX-10	500
MAX11154	18	0 to 5	Internal/External	3mm x 3mm TDFN-12	500
MAX11156	18	±5	Internal/External	3mm x 3mm TDFN-12	500
MAX11158	18	±5	Internal	3mm x 5mm µMAX-10	500

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11161EUB+	-40°C to +85°C	10 µMAX
MAX11161EUB+T	-40°C to +85°C	10 µMAX

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	**21-0061**	**90-0330**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/15	Initial release	—

