EVBUM2260/D

KAF-8300 Evaluation Timing Specification

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

The Altera code described in this document is intended for use in the AD984X Timing Board. The code is written specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit:	PN 4H0475
Timing Generator Board	3E8092 (AD9845A 28 MHz)
KAF−8300 Imager Board	3E8360
Framegrabber Board	National Instruments model PCI−1424

ALTERA CODE FEATURES / FUNCTIONS

The Altera Programmable Logic Device (PLD) has three major functions:

Timing Generator

The PLD serves as a state machine−based timing generator whose outputs interface to the KAF−8300, the AD9845A Analog Front End (AFE), and the PCI−1424 Framegrabber. The behavior of these output signals is dependent upon the current state of the state machine. External digital inputs, as well as jumpers on the board can be used to set the conditions of certain state transitions (See Table 2). In this manner, the board may be run in any of the following operating modes:

- Three Different Image Capture Modes:
  - Single Capture Mode using an External Trigger (Still Mode)
  - Continuous Capture Free−Run Mode
  - Continuous Capture Still−Run Mode
- 32 different Pre−defined Integration Mode Options
- External Custom Integration Time Option
- Pulsed or Non−pulsed INTEGRATE Output Sync Options
- Nominal or Extended Clocking Mode Option
- Four different AFE Optical Black Clamp (CLPOB) Modes

Delay Line Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD programs the 10 silicon delay IC's on the Timing Generator Board to their default delay settings via a 3 wire serial interface. See Table 12 for details.

AFE Register Initialization

Upon power up, or when the BOARD_RESET button is pressed, the PLD programs the registers of the two AFE chips on the Timing Generator Board to their default settings via a 3 wire serial interface. See Table 13 for details.

ALTERA CODE I/O

Table 2. INPUTS

Symbol	Description
POWER_ON_DELAY	The rising edge of this signal clears and re−initializes the PLD
SYSTEM_CLK	56 MHz clock, 2X the desired pixel clock rate
INTEGRATE_CLK	(Provides 1 ms unit integration time)
JMP[1..0]	Output mode select: JMP1 JMP0 Output Mode 0 X Free−Running Mode 1 0 Still Mode (requires external trigger) 1 1 Still/Run Mode
JMP2	Internal/External Integration Control Mode HIGH = External Integration Control using DIO13 LOW = Pre−Set Internal Integration Settings in conjunction with DIO[10..6]
JMP3	Overclock Timing Mode HIGH = Extended Overclock Testing LOW = Nominal Timing
DIO[1..0]	AD9845A CLPOB Mode control lines (See Table 10)
DIO[5..2]	Pulse INTEGRATE output control lines
DIO[10..6]	Integration Time control lines (See Table 11)
DIO11	Asynchronous Reset Control Line
DIO12	Remote capture control line (when Still operating mode selected)
DIO13	User defined integration time control line (when External INT mode selected)
DIO[19..14]	(Not used for ‘Error! Auto Text entry not defined.’ operation)

Table 3. OUTPUTS

Symbol	Description
V1_CLK	Error! AutoText entry not defined. V1 Clock
V2_CLK	Error! AutoText entry not defined. V2 Clock
H1_CLK	Error! AutoText entry not defined. H1 Clock
H1BR_CLK	Error! AutoText entry not defined. H1L Clock
H2_CLK	Error! AutoText entry not defined. H2 Clock
R_CLK	Error! AutoText entry not defined. Reset Clock
SHP	AD9845A Clamp CCD Reset Level
SHD	AD9845A Sample CCD Data Level
DATACLK	AD9845A A/D Convert Clock
PBLK	AD9845A Pixel Blanking
CLPOB	AD9845A Black Level Clamp
CLPDM	AD9845A DC Restore Input Clamp
VD	(not used for KAF−8300)
HD	(not used for KAF−8300)
PIX	PCI−1424 Frame Grabber Pixel Rate Synchronization
FRAME	PCI−1424 Frame Grabber Frame Rate Synchronization
LINE	PCI−1424 Frame Grabber Line Rate Synchronization
CH1_SLOAD	Serial Load Enable, Ch1 AD9845A AFE
CH2_SLOAD	Serial Load Enable, Ch2 AD9845A AFE

Table 3. OUTPUTS

Symbol	Description
SLOAD	Serial Load Enable, Delay Line IC's
SCLOCK	Serial Clock (AD9845A, Delay Line IC's)
SDATA	Serial Data (AD9845A, Delay Line IC's)
FDG	(not used for KAF−8300)
INTEGRATE	High (or pulsed) during CCD Integration Time
V3RD	(not used for KAF−8300)
V_SHUTTER	(not used for KAF−8300)
V2B_CLK	(not used for KAF−8300)
H2BR_CLK	(not used for KAF−8300)

KAF−8300 TIMING CONDITIONS

Table 4. SYSTEM TIMING CONDITIONS

Description	Symbol	Time	Notes
System Clock Period	Tsys	17.86 ns	56 MHz system clock
Unit integration time	Uint	1 ms	Typical
Power stable delay	Tpwr	30 ms	Typical
Default Serial Load Time	Tsload	192 μs	Typical

Table 5. CCD TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
H1, H2, RESET period	Tpix	35.71 ns	1	28 MHz clocking of H1, H1L, H2, RESET
VCCD delay	Tvd	35.71 ns	1	Between Hclks stopping and V1 rising edge
Horizontal setup time	Ths	1.0 μs	28	Between V2 falling edge and Hclks startup
Vertical transfer period	Vperiod	9.07 μs	254	Vperiod = Tvd + TVCCD + Ths
VCCD transfer time	TVCCD	8.0 μs	224	Between V1 rising edge and V2 falling edge
Pixels per line	PIX_X	123.63 μs	3462	3448 CCD pixels (3326 active) plus 14 overlock
Lines per frame	PIX_Y		(2584)	2574 CCD lines (2504 active) plus 10 overlock lines
RESET clock pulse width	Tr	5.0 ns		Tr is set by hardware on imager board
Vertical flush period	Fperiod	8.11 μs	227	Time to flush one line
Flush duration	Flines		(2638)	Number of lines flushed = 2638 (2574 + 64 extra)
Flush delay	Fdelay	0−1 ms		Variable due to synchronization with Integration Clock
Flush time	Ftime	~22 ms		Ftime = (Fperiod x Flines) + Fdelay

Table 6. AFE TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
SHP,SHD,DATACLK period	Tpix	35.71 ns	1	28 MHz clocking of SHP,SHD,DATACLK
SHP pulse width	Tshp	7.5 ns		Tshp is set by hardware on timing board
SHD pulse width	Tshd	7.5 ns		Tshd is set by hardware on timing board
CLPOB1 line start	CLPOB1_ls		5	Line transfer counter, CLPOB modes 0,2 only
CLPOB1 line end	CLPOB1_le		15	Line transfer counter, CLPOB modes 0,2 only

Table 6. AFE TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
CLPOB1 start pixel	CLPOB1_ps		200	Line transfer counter, CLPOB modes 0,2 only
CLPOB1 end pixel	CLPOB1_pe		2500	Line transfer counter, CLPOB modes 0,2 only
CLPOB2 start pixel	CLPOB2_ps		3450	Line transfer counter, CLPOB modes 0,1 only
CLPOB2 end pixel	CLPOB2_pe		3454	Line transfer counter, CLPOB modes 0,1 only
CLPDM start pixel	CLPDM_ps		3456	Horizontal transfer counter
CLPDM end pixel	CLPDM_pe		3460	Horizontal transfer counter
PBLK start pixel	PBLK_ps		1	Vertical transfer counter
PBLK end pixel	PBLK_pe		240	Vertical transfer counter

Table 7. PCI−1424 TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
Pixel period	Tpix	35.71 ns	1	28 MHz clocking of PIX sync signal
LINE START Delay	LSdel	321.4 ns	9	Delay 9 clocks for AFE pipeline delay (See Figure 10)
LINE END delay (Normal Mode)	LEdel	35.71 ns	1	End of previous line (See Figure 10)
LINE END delay (Extended Mode)	LEdel	1.0 μs	28	End of previous line (See Figure 10)
FRAME time (Normal Mode)	Tframe	342.9 ms	9,601,890	Tframe = Tpix * ((Vperiod + PIX_X) * (PIX_Y − 1) + + PIX_X)
FRAME time (Extended Mode)	Tframe	370.3 ms	10,368,358	Tframe = Tpix * ((Vperiod + PIX_X) * (PIX_Y − 1) + + PIX_X)

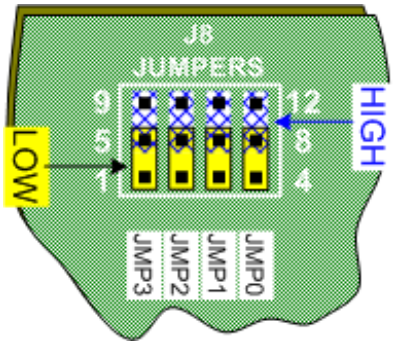

Figure 1. Timing Board J8 Jumpers

MODES OF OPERATION

The following modes of operation are available to the user.

Output Modes

The output mode is selected by setting the JMP[0..3] inputs to the appropriate level (See Figure 1 and Table 8)

Table 8. OUTPUT MODE JUMPER SETTINGS

JMP3	JMP2	JMP1	JMP0	Binning Mode Operation
		HIGH	LOW	Still Mode
		HIGH	HIGH	Still/Run Mode
		LOW	X	Free−Run Mode
	LOW			Pre−Set INT settings selected with DIO[10..6]
	HIGH			External INT control using DIO13
LOW				Extended Overclock Image Dimensions
HIGH				Nominal Image Dimension

Integration Modes

The integration time can be controlled in one of two ways:

1. To select the external integration time mode, Set JMP2 high. External integration mode requires an external input via the digital input interface to be synchronized with the timing board to create any number of custom integration times. The rising edge of the external input ends the integration time.
2. To select the internal integration time mode, Set JMP2 low. In Internal integration mode, the unit integration clock timer and the digital input interface (DIO[10..6]) are used to select one of thirty two different pre−defined integration times.

Each of the pre−defined integration times is a multiple of the Unit integration time. See Table 11.

Pulsed Integration Mode

The INTEGRATE output sync signal can either be set high for the duration of the desired integration time period or it can be pulsed on and off for a number of cycles. When using the pulsed INTEGRATE option the output pulse will have a 2 ms period, 50% duty cycle (for the first ms the pulse is low, for the second ms the pulse is high). The number of pulses are specified via DIO [5..2] (See Table 9). For proper operation, the user must be sure to set the integration time to be equal to or greater than the number of pulses selected times the 2 ms pulse period.

Table 9. PULSE MODE SETTINGS

Pulse Mode DIO[5..2]	Number of Pulses
0	ALWAYS HIGH
1	1
2	2
3	3
4	4
5	5
6	10
7	20
8	30
9	40
10	50
11	75
12	100
13	150
14	200
15	ALWAYS LOW

Black Clamp Modes

One of the features of the AD9845A AFE chip is an optical black clamp. The black clamp (CLPOB) is asserted during the CCD's dark pixels and is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. Several options for operating this black clamp are provided and are controlled by the digital inputs D[13..12] (See Table 10). The default CLPOB mode is 0.

Table 10. BLACK CLAMP MODES

CLPOB Mode DIO[1..0]	Black Clamp Operation	Notes
0	CLPOB asserted several dark lines per frame, and several dark pixels per line	Default Mode
1	CLPOB asserted several dark pixels per line	
2	CLPOB asserted several dark lines per frame	
3	Off, CLPOB always held high	

Table 11. PRE−SET INTEGRATION TIMES

INT Mode DIO[10..6]	Integration Time (ms)
0	1
1	2
2	3
3	4
4	5
5	7
6	10
7	14
8	19
9	23
10	39
11	67
12	89
13	100
14	125
15	150
16	189
17	200
18	250
19	300
20	322
21	400
22	489
23	739
24	989
25	1489
26	1989
27	4989
28	9989
29	14989
30	29989
31	59989

PIXEL RATE CLOCKS GENERATION

The pixel rate clocks are derived from the system clock. They operate at 1/2 the frequency of the system clock. The PIXEL_CLK signal is generated from the rising edge of the system clock. The DELAYED_PIX_CLK signal is generated from the falling edge of the system clock. By utilizing both edges of the system clock, four start positions for the pixel rate clocks are achieved:

1. The PIXEL_CLK signal
2. The DELAYED_PIX_CLK signal occurs 25% later than the PIXEL_CLK signal
3. The inverse of the PIXEL_CLK signal occurs 50% later than the PIXEL_CLK signal
4. The inverse of the DELAYED_PIX_CLK signal occurs 75% later than the PIXEL_CLK signal

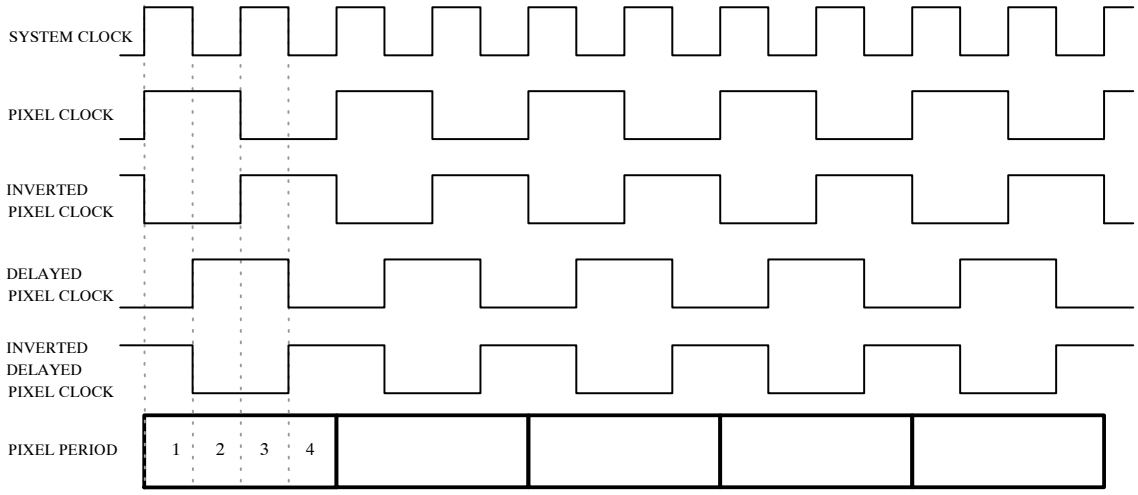

Figure 2. Pixel Clock Generation Timing

One of these four signals is chosen to be the input signal source for a particular pixel rate signal, and then the position of the signal is optimized using a programmable delay line IC.

TIMING GENERATOR STATE MACHINE DESCRIPTION

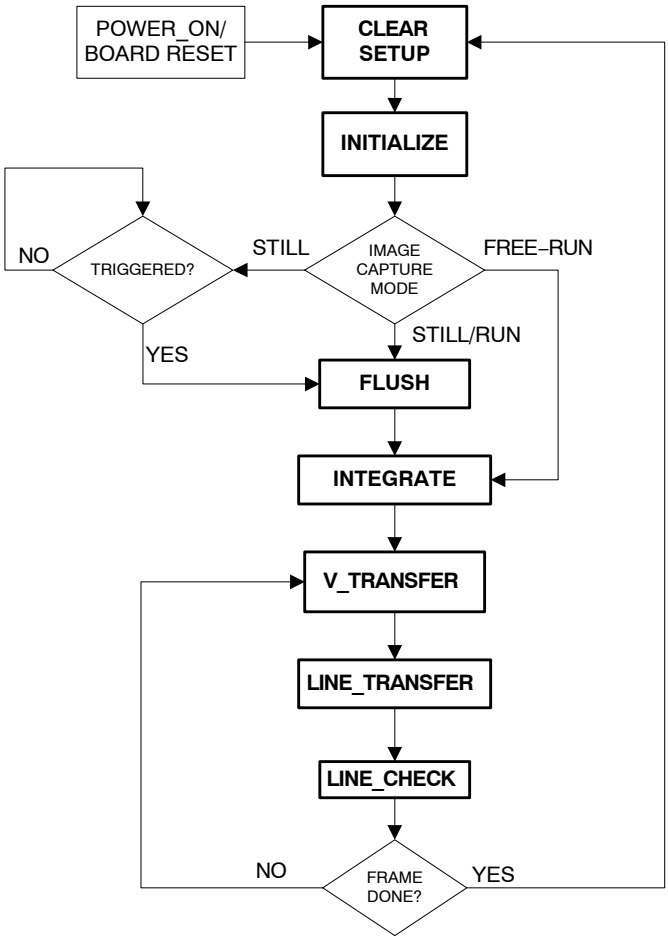

Figure 3. Timing Generator State Machine

Power−On / Board Reset State

When the board is powered up or the Board Reset button is pressed, the Altera PLD is internally reset. When this occurs, state machines in the PLD will first serially load the initial default values into the ten delay line IC's on the board, and then serially load the initial default values into the AFE registers. Upon completion of the serial load of the AFE, the board will be ready to proceed according to the output mode selected.

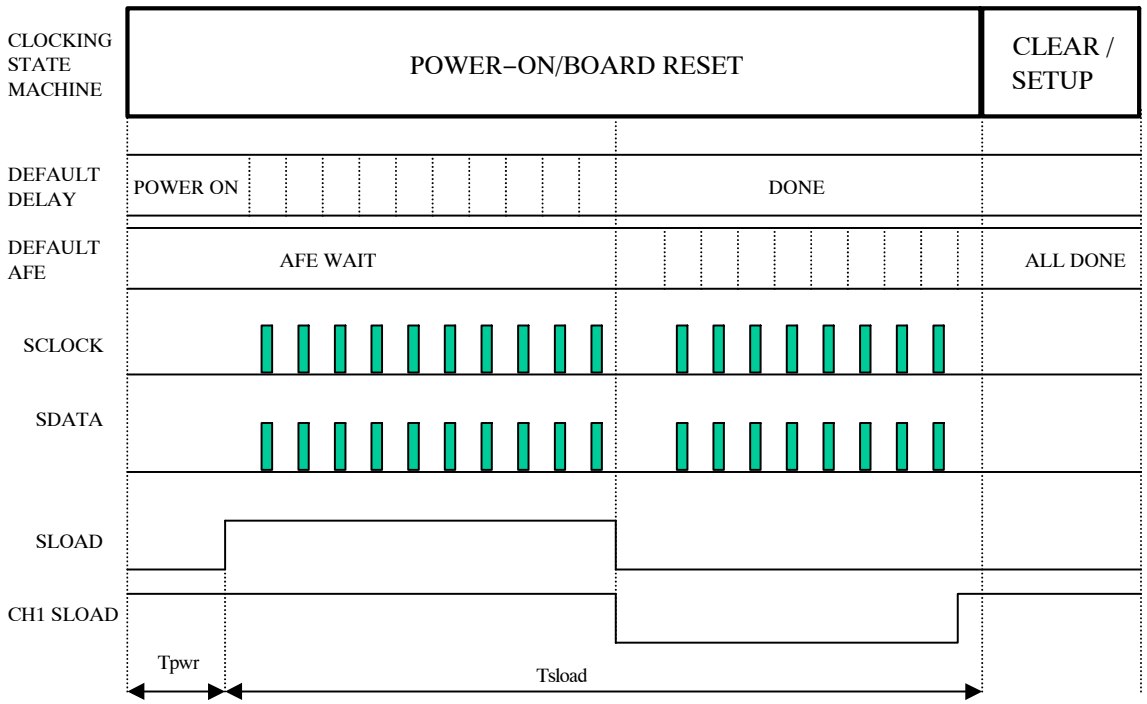

Figure 4. Power on Initialization Timing

Delay Register Initialization

The DS1020 Programmable Silicon Delay Lines allow the Horizontal Clocks, Reset Clock, Clamp, Sample, and Data Clock signals to be adjusted within the sub−pixel timing. On Power−Up or Board Reset, the delay lines are programmed with values stored in the Altera device. These values are chosen to comply with the timing requirements of the CCD image sensor (See the References for details). The delay values shown in Table 12 are typical values, and may vary on an individual Evaluation Board set.

For programming purposes, the silicon delay lines are cascaded, i.e., the serial output pin of device 1 is tied to the serial input pin of device 2 and so on. Therefore, when making an adjustment to one or more delay lines, all the delay lines must be reprogrammed. The total number of serial bits must be eight times the number of units daisy−chained and each group of 8 bits must be sent in MSB−to−LSB order (See References). The total delay on each output signal is calculated as:

$$Delay = 10.0 + 0.25 * [Delay\ Code] \text{ (ns)}$$

Refer to the Dallas Semiconductor DS1020 Programmable Silicon Delay Line Specification Sheet (References) for details.

Table 12. DEFAULT DELAY IC PROGRAMMING

Programming Order	Delay IC Output Signal	Delay IC Input Signal Source	Delay Code (Typical)	Delay (ns) (Typical)
1	AD9845A DATACLK	DELAYED PIXEL CLK	0	10.00
2	CH2 AD9845A SHP	(not used)	32	18.00
3	CH1 AD9845A SHP	PIXEL CLK	22	15.50
4	CH2 AD9845A SHD	(not used)	48	22.00
5	CH1 AD9845A SHD	DELAYED PIXEL CLK	38	19.50
6	H1 CLOCK	PIXEL CLK	16	14.00
7	H1BR CLOCK	PIXEL CLK	16	14.00
8	H2 CLOCK	PIXEL CLK	16	14.00
9	H2BR CLOCK	(not used)	16	14.00
10	RESET CLOCK	INVERTED DELAYED PIXEL CLK	30	17.50

AFE Register Initialization

On power up or board−reset, the AFE registers are programmed to the default levels shown in Table 13. See the AD9845A specifications sheet (References) for details.

Table 13. DEFAULT AD9845A AFE REGISTER PROGRAMMING

Register	Description	Value (decimal)	Notes
0	Operation	128	
1	VGA Gain	267	Corresponds to a VGA stage gain of 7.1 dB
2	Clamp	200	The output of the AD9845A will be clamped to code 200 during the CLPOB period
3	Control	10	CDS gain enabled
4	CDS Gain	43	Corresponds to a CDS stage gain of 0.0 dB

CLEAR / SETUP and INITIALIZE States

The timing generator state machine is free running. It cycles through the states depending on the jumper settings and DIO inputs, and then returns back to the clear/setup state to begin the next frame. The clear/setup state is used to reset the internal PLD counters at the beginning of each frame. The INITIALIZE state is used to determine the selected operating modes, and to synchronize with the INTEGRATE_CLK as needed. The state machine will wait in the INITIALIZE state for the next rising edge of INTEGRATE_CLK (See Figure 6).

FLUSH State

During the FLUSH state, the CCD is flushed of any accumulated charge by running the vertical clocks continuously for a number of lines. Upon flush completion, the state machine will wait in the flush state until the next rising edge of the INT_CLK. The reason for the delay before entering the INTEGRATE state is so that state machine is re−synchronized with the INT_CLK after the asynchronous external trigger, ensuring that consistent integration times are achieved when using the pre−defined internal integration modes (See Figure 5 and Table 11).

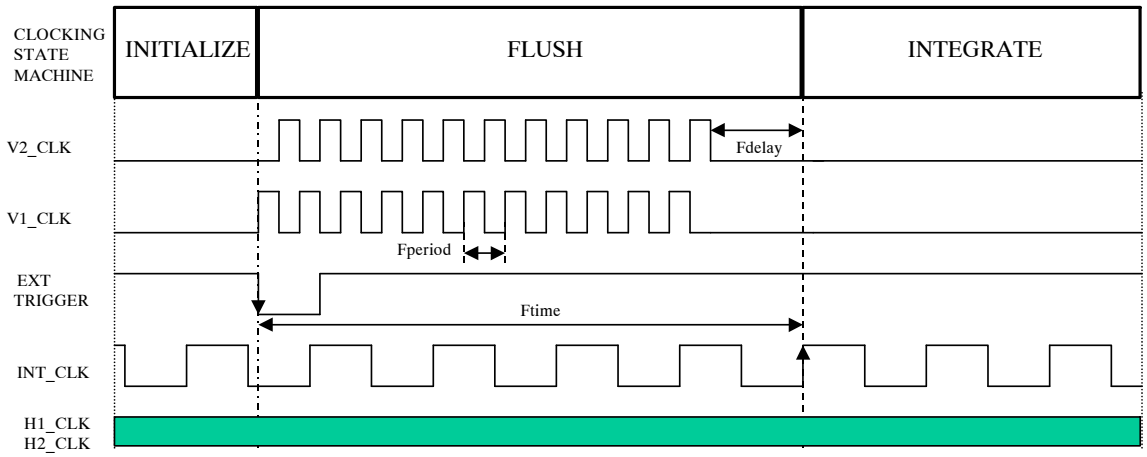

Figure 5. Still Mode Flush Timing

INTEGRATE State

Normal Integration

During the INTEGRATE state, there is a delay of 2 INT_CLK periods (Int Delay1) before the output signal INTEGRATE goes high. INTEGRATE stays high a pre−defined multiple of the unit integration time depending on the digital inputs D[10..6] (See Table 10). There is a fixed delay of 2 INT_CLK periods (Int Delay2) after INTEGRATE goes low, before the INTEGRATE state is exited and V_TRANSFER begins.

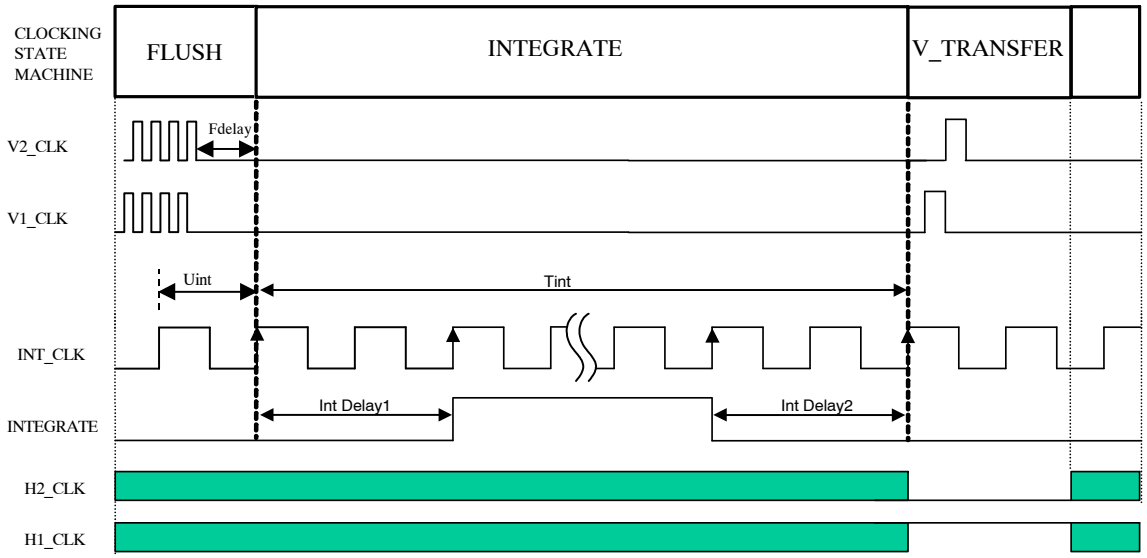

Figure 6. Normal Integration Timing

Pulsed Integration

In Pulsed Integration Mode, the INTEGRATE signal may be pulsed a preset number of times without altering the Integration Timing. The pulses are 1 Unit Integration wide, and the pulse period is 2 Unit Integration times. The number of pulses issued is controlled by DIO[5..2] (See Table 9). By default (Normal Integration), INTEGRATE is always on during the entire Integration window; alternatively from 0 to 200 pulses may be issued. For proper operation, the user must be sure to set the INTEGRATE window to be equal to or greater than twice the number of pulses selected.

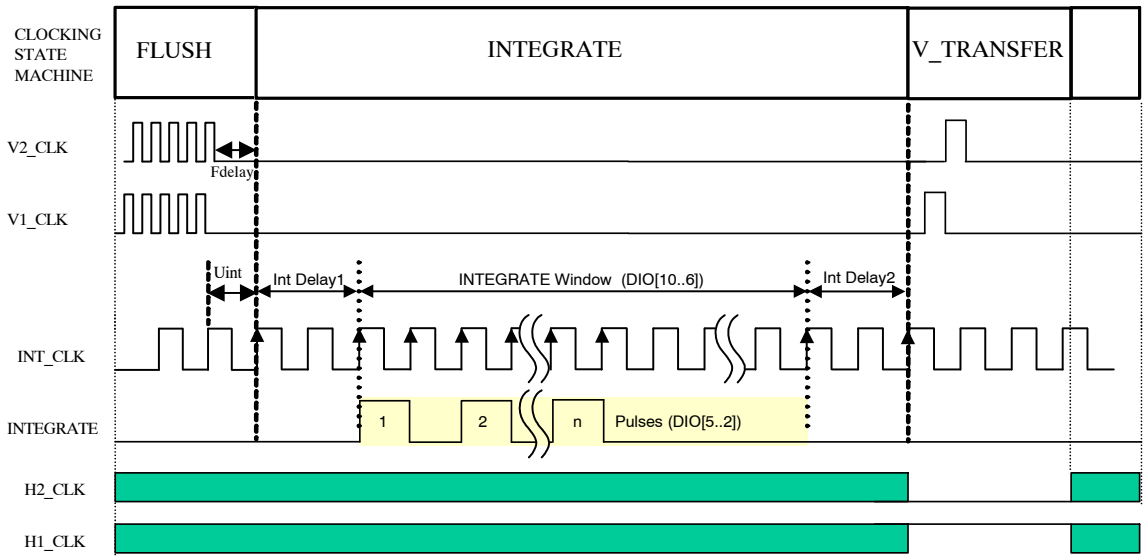

Figure 7. Pulsed Integration Timing

V_TRANSFER State

During the V_TRANSFER state, each line (row) of charge is transported towards the horizontal CCD register using the Vertical clocks. A vertical transfer counter in the PLD is used to determine when the vertical clocks are forced high and low and when the vertical transfer time and horizontal delay time (T_{hs}) are completed.

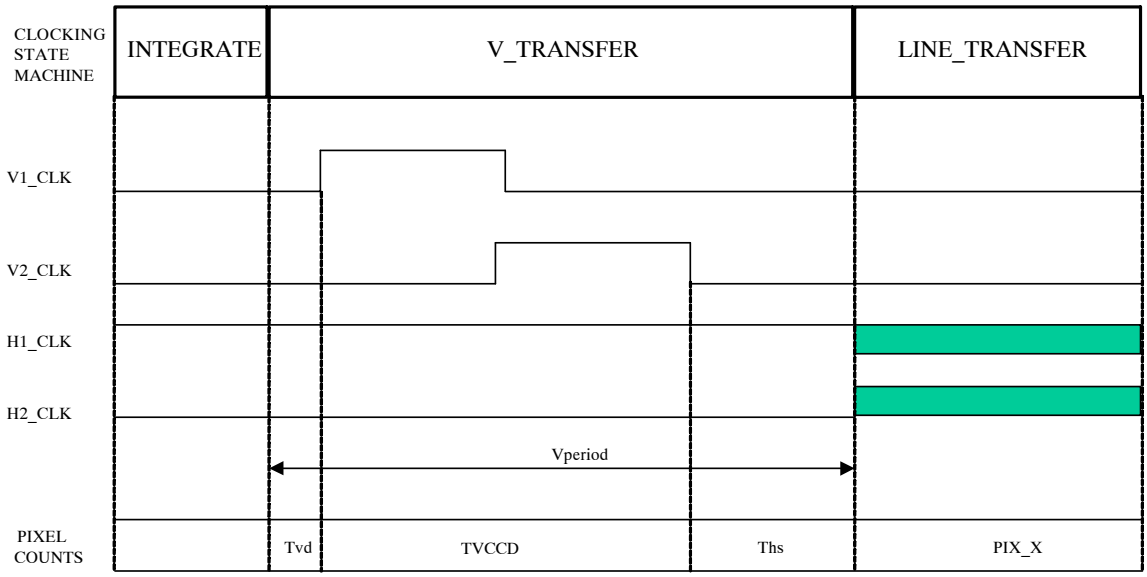

Figure 8. Vertical Transfer Timing

LINE_TRANSFER and LINE_CHECK State

During the LINE_TRANSFER state, charge is transported to the CCD output structure pixel by pixel. A line transfer counter in the PLD is used to keep track of how many pixels have been transported, and to synchronize the AD9845A timing signals and the PCI−1424 timing signals with the appropriate pixels (dark pixels for black clamping, for example).

At the end of each line transfer, the Line counter is incremented in the LINE_CHECK State. If all of the lines have been clocked out of the CCD, the state machine goes to the CLEAR/SETUP state; if not, the state machine returns to the V_TRANSFER state, and transfers another line of charge into the horizontal register.

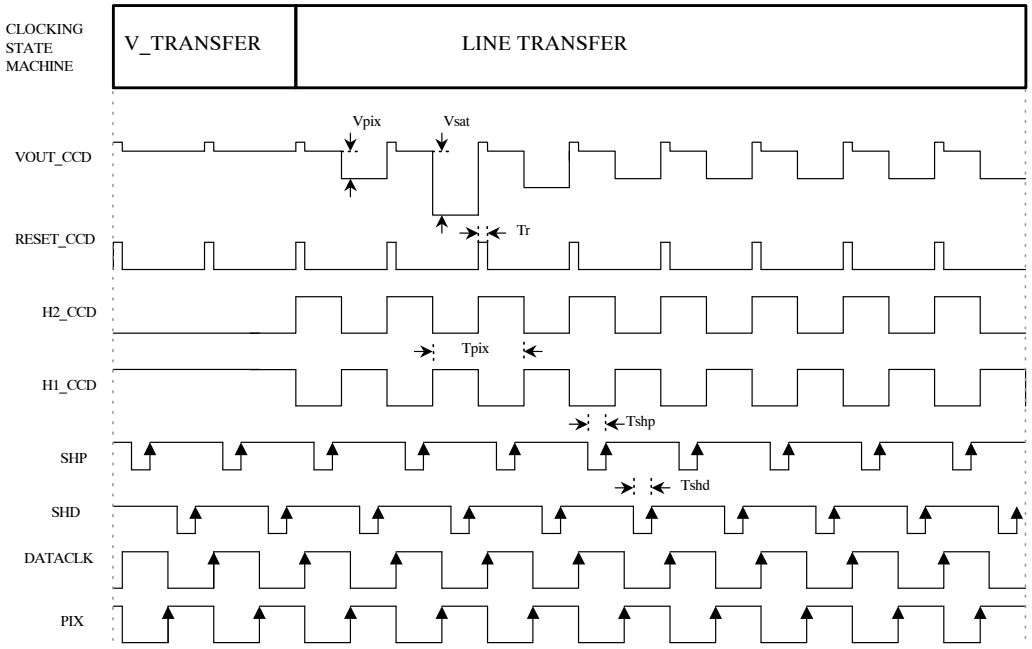

Figure 9. Horizontal Timing – Line Transfer

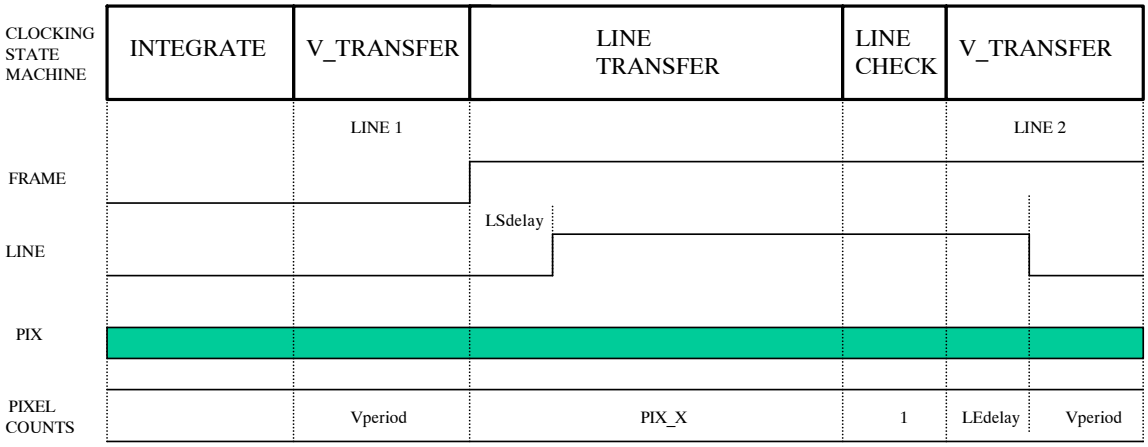

Figure 10. PCI−1424 Frame Grabber Timing

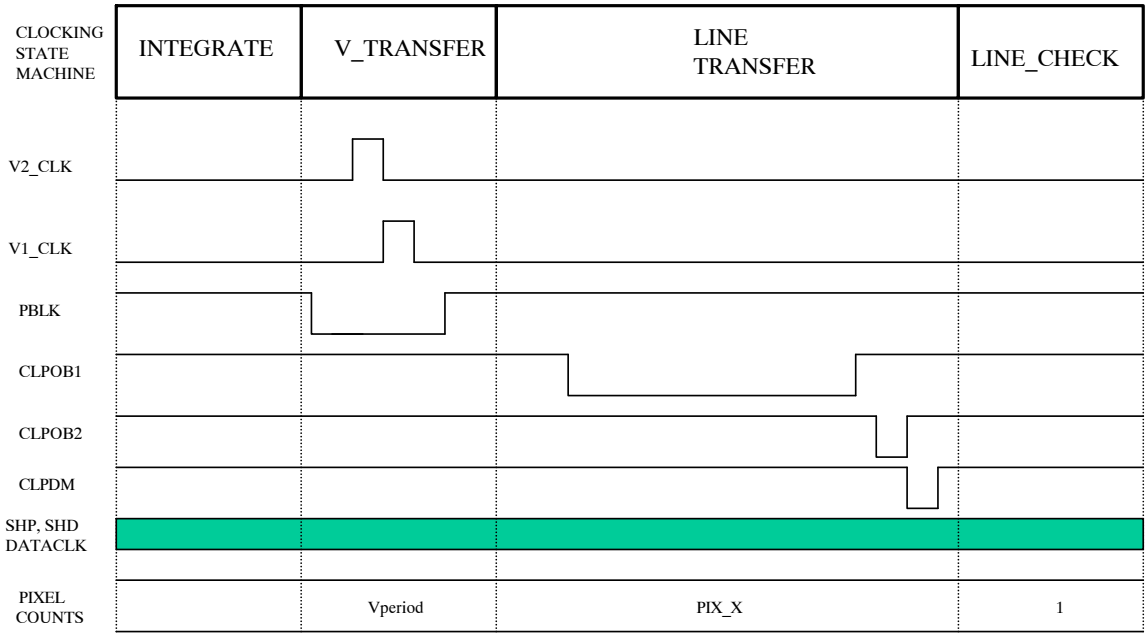

Figure 11. AD9845A Timing

VIDEO SIGNAL PATH

The entire video signal path through the Imager Board and Timing Board is represented in Figure 12. The individual blocks are discussed in the Imager Board User Manual and the Timing Board User Manual.

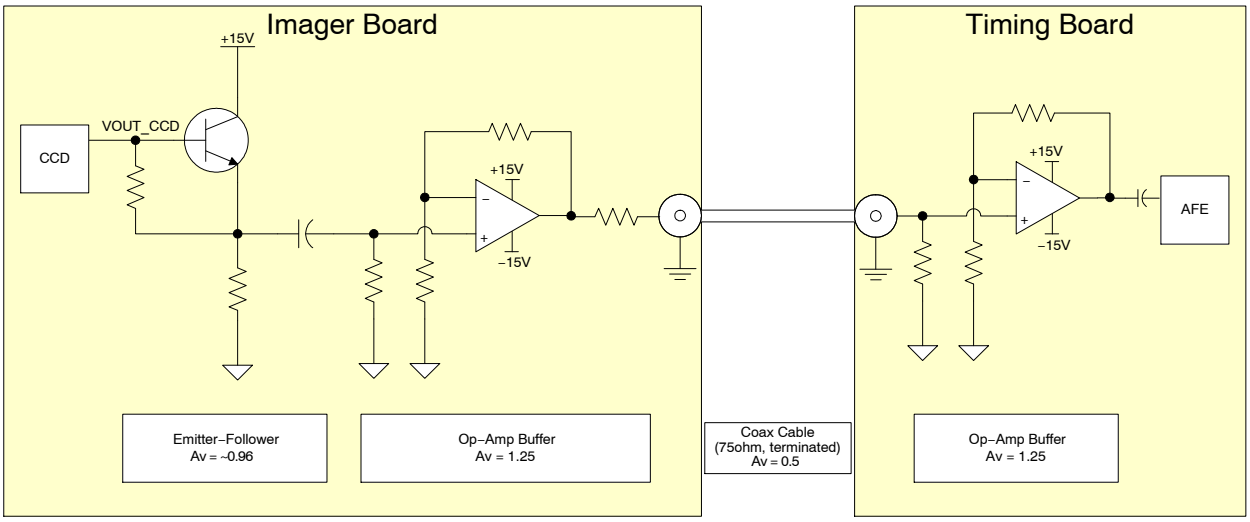

Figure 12. Video Signal Path Diagram

The gain for the entire signal path can be calculated by multiplying the gains of the individual stages:

$0.96 \times 1.25 \times 0.5 \times 1.25 = 0.75$

The gain of the entire signal path is designed so that the AFE input is not overloaded (See References). The default AFE programmable gain settings (See Table 13) are designed to maximize the dynamic range of the AFE.

Warnings and Advisories

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615
Phone: (585) 784−5500
E−mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

References

- KAF−8300 Device Specification
- KAF−8300 Imager Board User Manual
- KAF−8300 Imager Board Schematic
- AD984X Timing Generator Board User Manual
- AD984X Timing Generator Board Schematic
- Analog Devices AD9845 Product Data Sheet (28 and 30 MHz operation)

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