PIC16F636/639

PIC16F636/639
Silicon Errata and Data Sheet Clarification

The PIC16F636/639 devices that you have received conform functionally to the current Device Data Sheet (DS41232**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F636/639 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision **(B4)**.

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2, MPLAB ICD 3, PICkit™ 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger, PICkit™ 2 or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Programmer>Select Tool*).
4. Perform a "Connect" operation to the device (*Programmer>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device ID values for the various devices and silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A1	B3	B4
PIC16F636	01 0000 101x xxxx	1	4	5
PIC16F639	01 0000 101x xxxx	1	4	5

Note 1: The device and revision data is stored in the Device ID located at 2006h in program memory.

2: Refer to the *"PIC12F6XX/16F6XX Flash Programming Specification"* (DS41204) for detailed information.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A1	B3	B4
Resets (Watchdog Timer)	WDT Reset	1.	Spurious Resets on prescaler modification.	X		
Wake-up Reset	Power-up Timer	2.	Time delay is skipped.	X		
Internal Oscillator/External Clock Switch Over	Internal/External Clock Switch Over	3.	Processor hangs in Reset if no oscillator.	X		
Data EEPROM	EEIF Flag Bit	4.	EEIF may be unintentionally cleared.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision **(B4)**.

1. Module: Resets (when WDT times out)

If the OPTION_REG bits, PS<2:0>, are changed from any other value to '000', multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

Work around

If a CLRWDT instruction is issued before the WDT times out and before the OPTION register PS<2:0> bits are modified, this problem is eliminated.

This issue was corrected in revision B silicon.

Affected Silicon Revisions

A1	B3	B4					
X							

2. Module: Wake-up Reset (WUR)

If a Wake-up Reset occurs when the Wake-up Reset (WURE) and Power-up Timer (PWTRE) Configuration bits are enabled in revision A silicon, there will not be a 72 ms time delay as expected.

Work around

There is no work around in revision A silicon for this errata. However, this issue was corrected for revision B silicon. If a Wake-up Reset occurs when the Wake-up Reset and Power-up Timer Configuration bits are enabled in revision B silicon, there will be a nominal 72 ms time delay following the Wake-up Reset.

Affected Silicon Revisions

A1	B3	B4					
X							

3. Module: Internal/External Clock Switch Over (IESO)

If a Wake-up Reset occurs when the Wake-up Reset (WURE) and Internal/External Clock Switch Over (IESO) Configuration bits are enabled in revision A silicon and there is no external clock applied to the chip when in the XT/HS configurations, the processor will hang on a Wake-up Reset.

Work around

There is no work around in revision A silicon for this errata. However, this issue was corrected for revision B silicon. If a Wake-up Reset occurs when the Wake-up Reset and Internal/External Clock Switch Over Configuration bits are enabled in revision B silicon and a Wake-up Reset occurs, the chip will wake up and reset as expected.

Affected Silicon Revisions

A1	B3	B4					
X							

4. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

Fix

Rev. B Silicon and later revisions.

Affected Silicon Revisions

A1	B3	B4					
X							

Data Sheet Clarifications

The following typographical corrections and clarifications are to be noted for the latest version of the device data sheet (DS41232**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module:

Increased maximum supply current for 20 MHz HS mode operation (D019).

15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Sym**	**Device Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
							VDD	**Note**
D019			—	2.6	**5.7**	mA	4.5	FOSC = 20 MHz HS Oscillator mode
			—	2.6	**5.7**	mA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

APPENDIX A: REVISION HISTORY

Rev A Document (8/2004)
Issue 1 – When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Added Clarifications/Corrections to the Data Sheet, Issues 1, 2 and 3 (changed to 8-pin MF **saw singulated** packaging).

Rev B Document (01/2005)

Added PIC16F639 device.

Revised Module 1: Resets.

Deleted Clarification/Corrections to the Data Sheet. Data Sheet has been updated.

Rev C Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 1: New 4x4 QFN Package added.

Rev D Document (02/2006)

Data Sheet Clarifications/Corrections Section: Added Module 2: I/O Pins.

Rev E Document (03/2006)

Data Sheet Clarifications/Corrections section: Added Module 3: Data EEPROM Memory; Added Module 4: Electrical Specifications. Replaced QFN Package Drawing.

Rev F Document (06/2006)

Added Module 2: “Wake-up Reset (WUR)”, and Module 3: “Internal/External Clock Switch Over”.

Rev G Document (11/2006)

Added Module 4: “Data EEPROM Memory”.

Data Sheet Clarifications/Corrections section: removed all sections, data sheet updated (DS41232**C**).

Rev H Document (06/2010)

Updated Errata to new format. Added Silicon Revisions A1, B3 and B4.

Data Sheet Clarification: Added Module 1.

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