PSMN020-30MLC

N-channel 30 V 18.1 mΩ logic level MOSFET in LFPAK33 using TrenchMOS Technology

4 September 2012 — Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising Superjunction technology
- Ultra low QG, QGD, and QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 1		-	-	31.8	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	33	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C; Fig. 10		-	20.5	27	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 10		-	14.7	18.1	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 5 A; V_{DS} = 15 V; Fig. 12; Fig. 13		-	1.7	-	nC
$Q_{G(tot)}$	total gate charge	V_{GS} = 4.5 V; I_D = 5 A; V_{DS} = 15 V; Fig. 12; Fig. 13		-	4.6	-	nC

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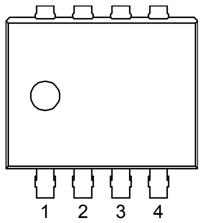
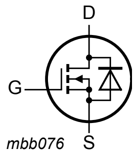
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN020-30MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1		-	31.8	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 1		-	22.5	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 4		-	127	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	33	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		130	-	V
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	27.4	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	127	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 31 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	7.7	mJ

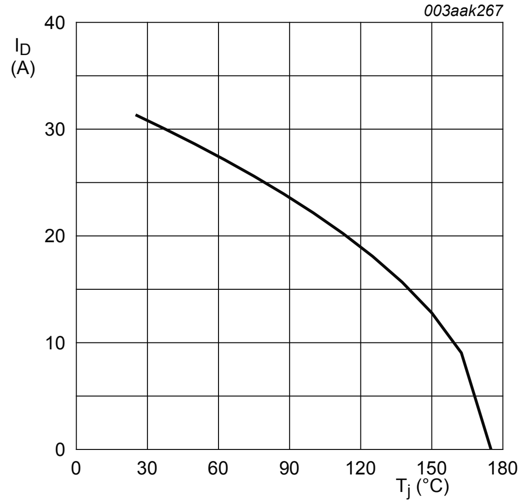


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

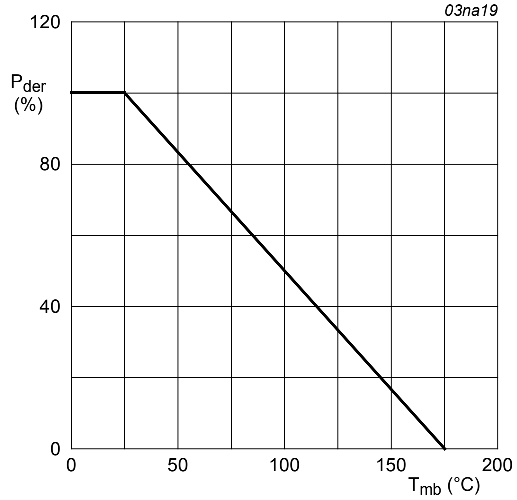


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

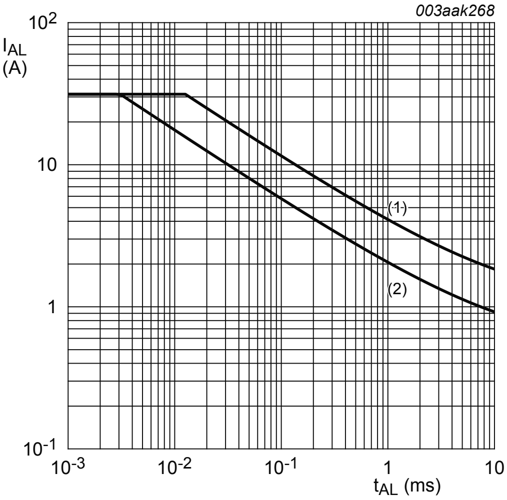


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

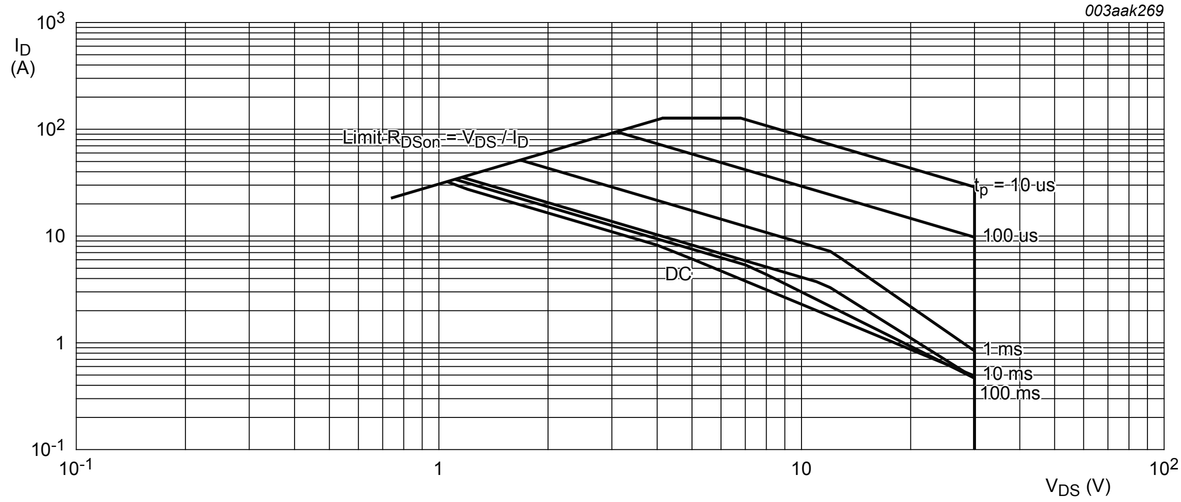


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25 °C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	4.32	4.56	K/W

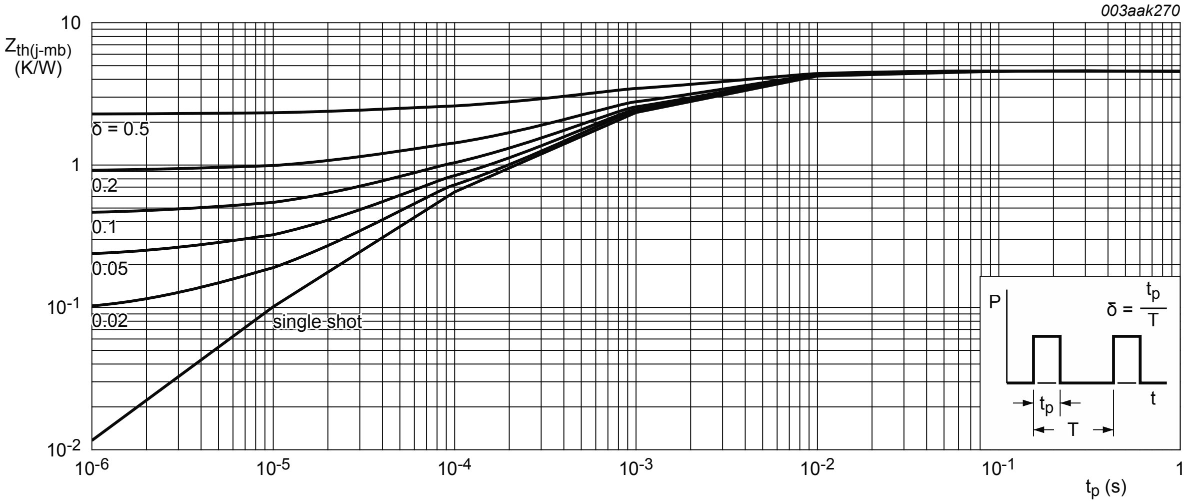


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 13.5 A; V_{GS} = 0 V; $T_{j(init)}$ = 25 °C; t_p ≤ 50 µs		34	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C		1.05	1.62	1.95	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature			-	-3.5	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C; Fig. 10		-	20.5	27	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	43.2	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 10		-	14.7	18.1	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	29	mΩ
R_G	gate resistance	f = 1 MHz		0.68	1.37	2.74	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	9.5	-	nC
		I_D = 5 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	4.6	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	8.4	-	nC
Q_{GS}	gate-source charge	I_D = 5 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	1	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	0.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.7	-	nC
Q_{GD}	gate-drain charge			-	1.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 5 A; V_{DS} = 15 V; Fig. 12; Fig. 13		-	2.4	-	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	430	-	pF
C_{oss}	output capacitance			-	120	-	pF
C_{rss}	reverse transfer capacitance			-	70	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 3 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	6.1	-	ns
t_r	rise time			-	7.2	-	ns
$t_{d(off)}$	turn-off delay time			-	10.1	-	ns
t_f	fall time			-	5.1	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_j = 25 °C		-	2.3	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.89	1.1	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V		-	13.5	-	ns
Q_r	recovered charge			-	5.1	-	nC
t_a	reverse recovery rise time	V_{GS} = 0 V; I_S = 5 A; dI_S/dt = -100 A/µs; V_{DS} = 15 V; Fig. 16		-	6.3	-	ns
t_b	reverse recovery fall time			-	7.2	-	ns

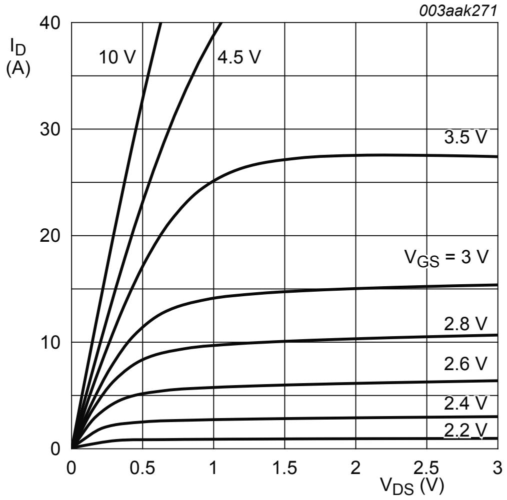


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

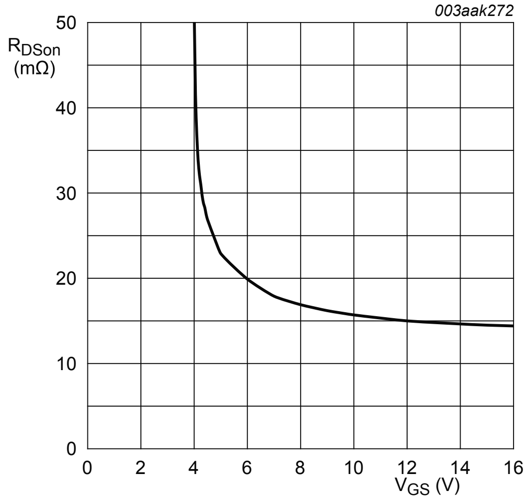


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 10A$

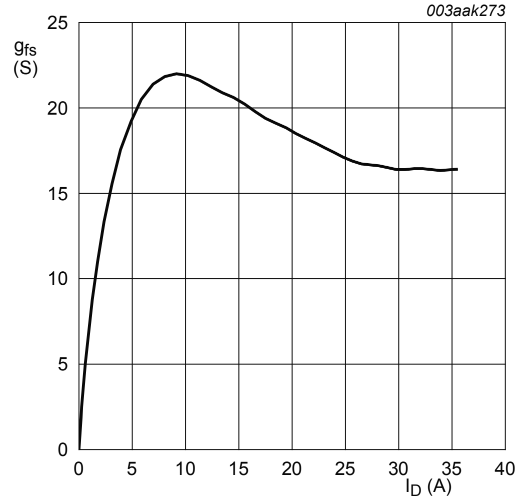


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

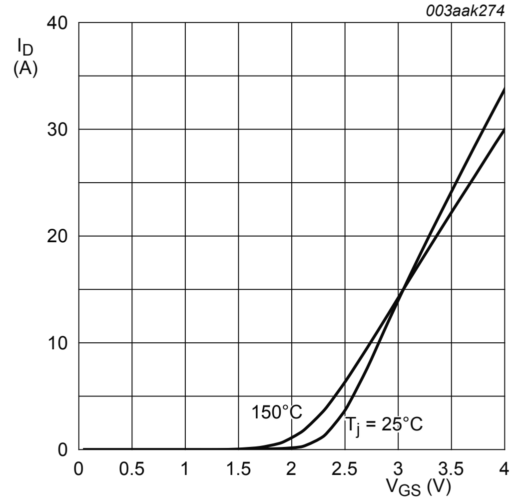


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

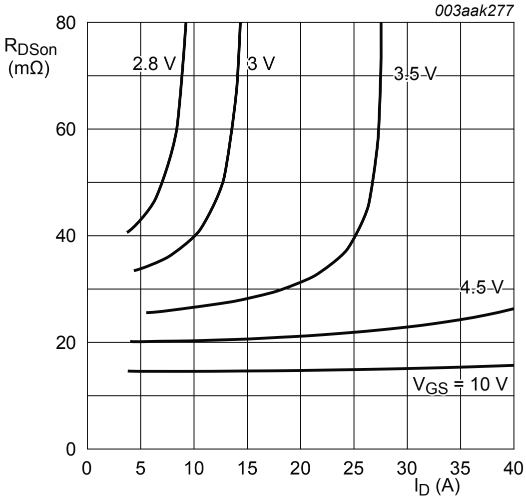


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

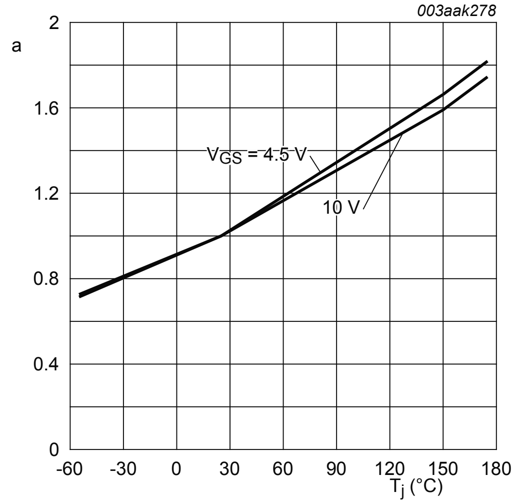


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

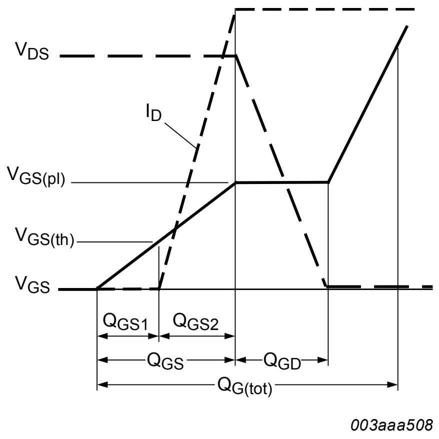


Fig. 12. Gate charge waveform definitions

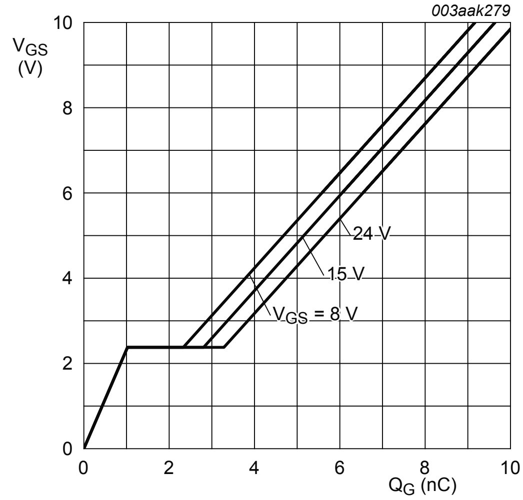


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 10A$

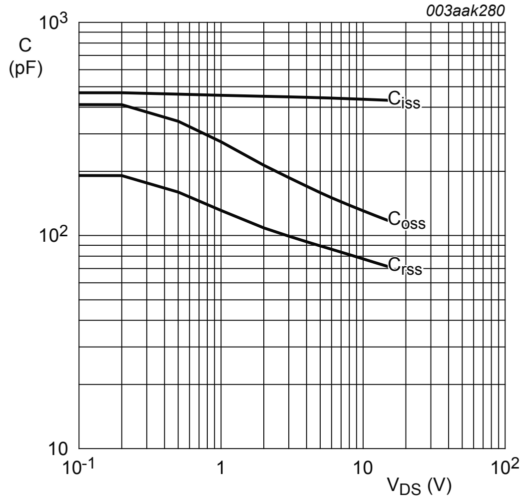


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

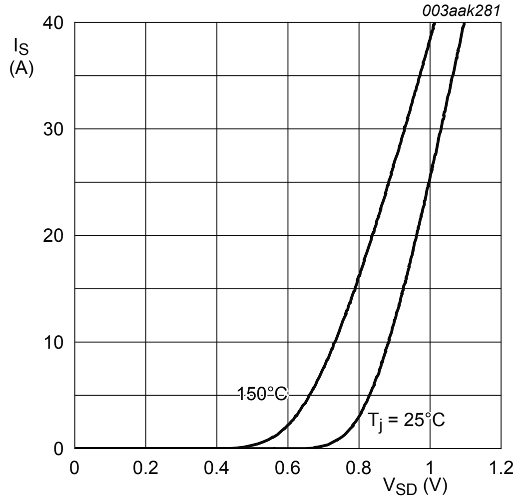


Fig. 15. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

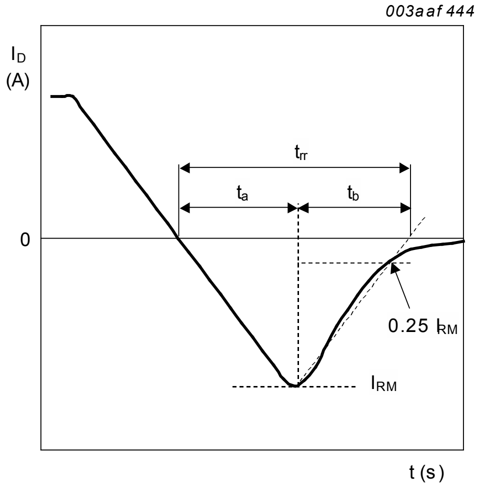
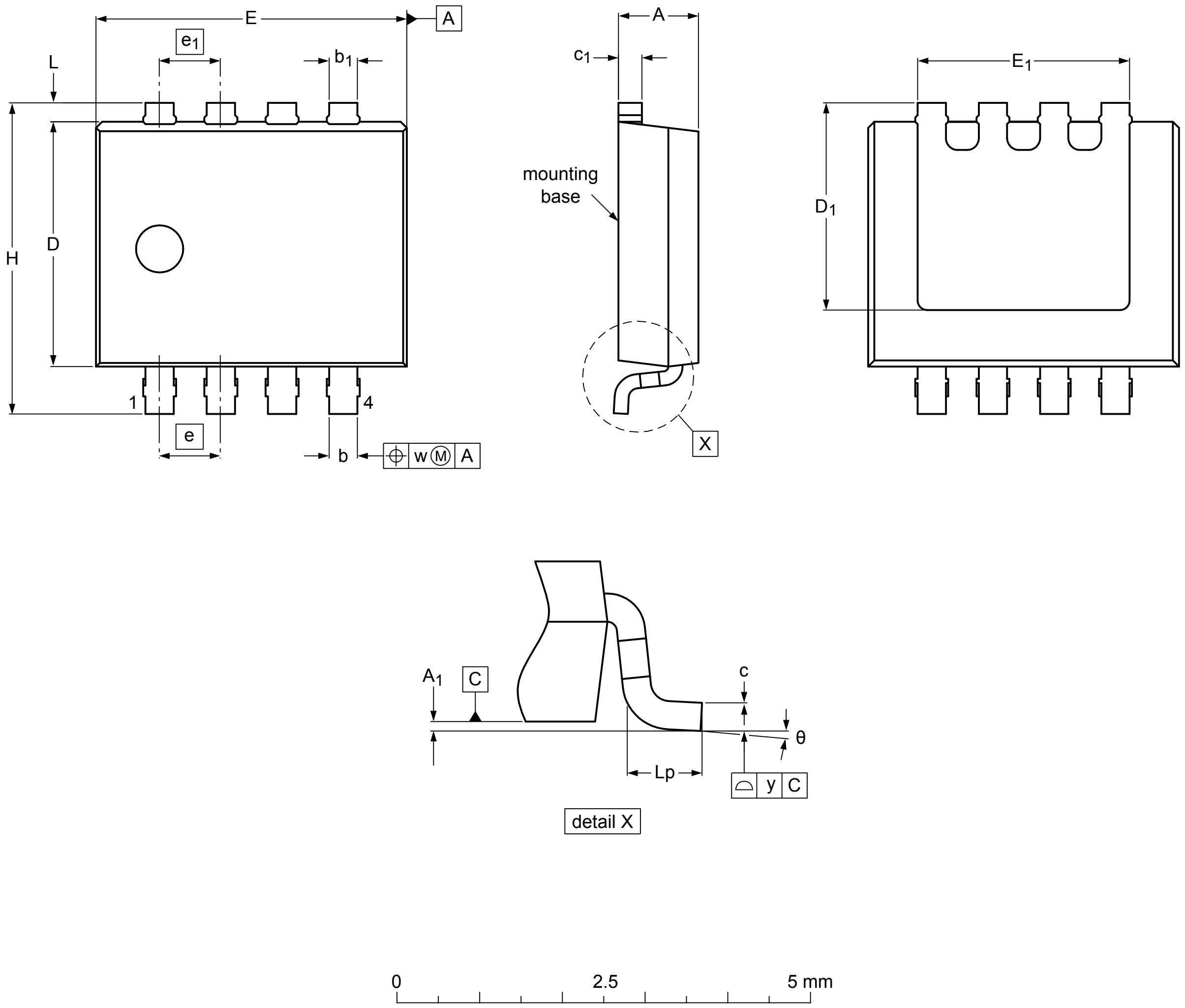


Fig. 16. Reverse recovery timing definition

7. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)		A	A_1	b	b_1	c	c_1	D(1)	D_1	E(1)	E_1	e	e_1	H	L	L_p	w	y	θ
mm	max	0.90	0.10	0.35	0.35	0.20	0.30	2.70	2.35	3.40	2.45			3.40	0.25	0.50			8°
	nom											0.65	0.65				0.20	0.10	
	min	0.80	0.00	0.25	0.25	0.10	0.20	2.50	1.90	3.20	2.00			3.20	0.13	0.30			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~11-12-19~~ 12-03-12

Fig. 17. Package outline LFPAK33 (SOT1210)

8. Legal information

8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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9. Contents