

XS1-L01A-TQ48 Datasheet

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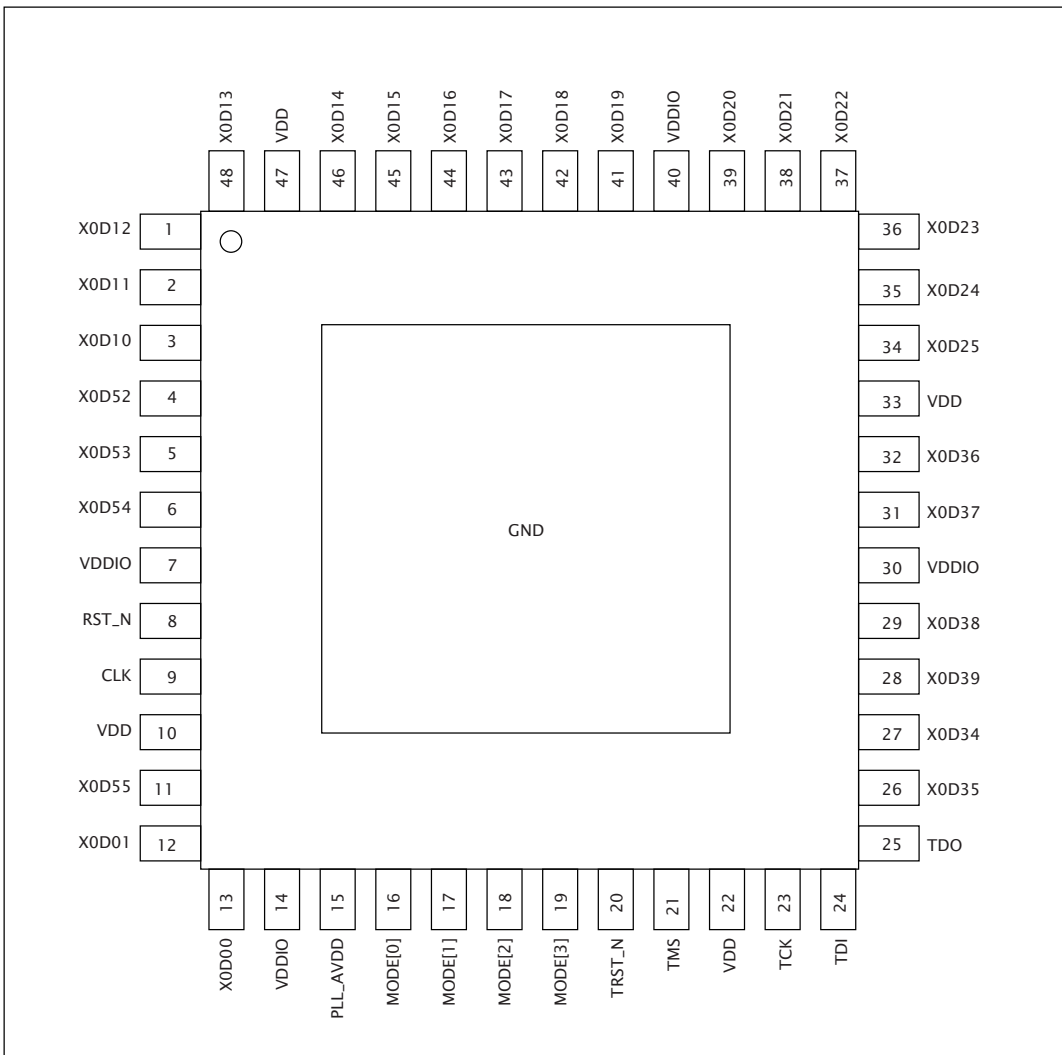
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1 Features

- ▶ **Single-Tile Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
 - Up to 500 MIPS shared between up to 8 real-time logical cores
 - Each logical core has:
 - Guaranteed throughput of between $\frac{1}{4}$ and $\frac{1}{8}$ of tile MIPS
 - 16x32bit dedicated registers
 - 159 high-density 16/32-bit instructions
 - All have single clock-cycle execution (except for divide)
 - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- ▶ **Programmable I/O**
 - 28 general-purpose I/O pins, configurable as input or output
 - Port sampling rates of up to 60 MHz with respect to an external clock
 - 32 channel ends for communication with other cores, on or off-chip
- ▶ **Memory**
 - 64KB internal single-cycle SRAM for code and data storage
 - 8KB internal OTP for application boot code
- ▶ **JTAG Module for On-Chip Debug**
- ▶ **Security Features**
 - Programming lock disables debug and prevents read-back of memory contents
 - AES bootloader ensures secrecy of IP held on external flash memory
- ▶ **Speed Grade**
 - 5: 500 MIPS
 - 4: 400 MIPS
- ▶ **Power Consumption**
 - Active Mode
 - 200 mA at 500 MHz (typical)
 - 160 mA at 400 MHz (typical)
 - Standby Mode
 - 14 mA
- ▶ **48-pin TQFP package 0.5 mm pitch**

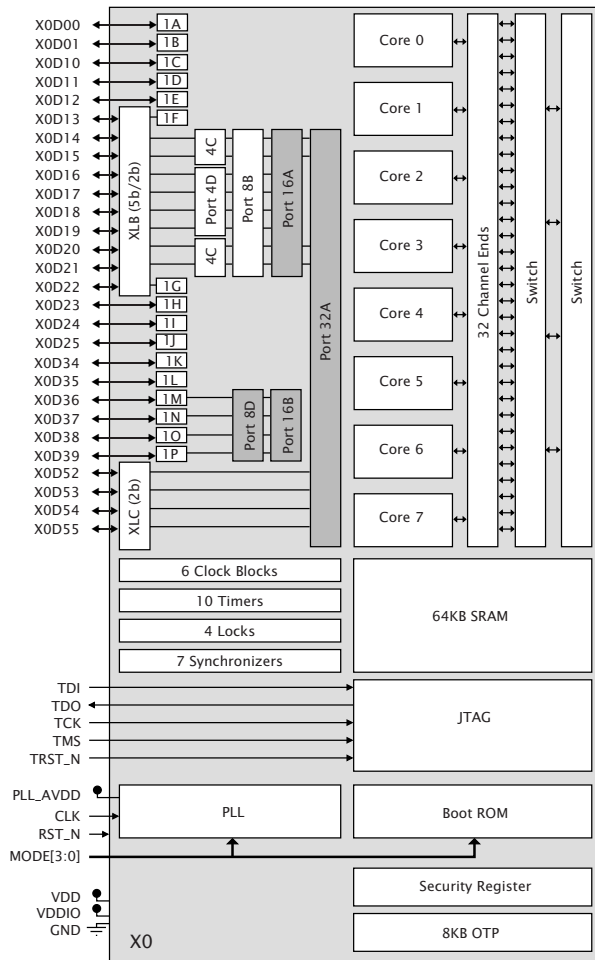
2 Pin Configuration



3 Signal Description

Module	Signal	Function	Type	Active	Properties
PU=Pull Up, PD=Pull Down, ST=Schmitt Trigger Input, OT=Output Tristate, S=Switchable R _S =Required for SPI boot (§5.6), R _U =Required for USB-enabled devices (§10)					
Power	GND	Digital ground	GND	—	
	VDD	Digital tile power	PWR	—	
	VDDIO	Digital I/O power	PWR	—	
	PLL_AVDD	Analog PLL power	GND	—	
	RST_N	Global reset input	Input	Low	PU, ST
PLL	CLK	PLL reference clock	Input	—	PD, ST
	MODE[3:0]	Boot mode select	Input	—	PU, ST
JTAG	TDI	Test data input	Input	—	PU, ST
	TDO	Test data output	Output	—	PD, OT
	TMS	Test mode select	Input	—	PU, ST
	TRST_N	Test reset input	Input	Low	PU, ST
	TCK	Test clock	Input	—	PU, ST
I/O	X0D00	P1A ⁰	I/O	—	PD _S , R _S
	X0D01	P1B ⁰	I/O	—	PD _S , R _S
	X0D10	P1C ⁰	I/O	—	PD _S , R _S
	X0D11	P1D ⁰	I/O	—	PD _S , R _S
	X0D12	P1E ⁰	I/O	—	PD _S , R _U
	X0D13	XLB ⁴⁰ _{5b} P1F ⁰	I/O	—	PD _S , R _U
	X0D14	XLB ³⁰ _{5b} P4C ⁰ P8B ⁰ P16A ⁸ P32A ²⁸	I/O	—	PD _S , R _U
	X0D15	XLB ²⁰ _{5b} P4C ¹ P8B ¹ P16A ⁹ P32A ²⁹	I/O	—	PD _S , R _U
	X0D16	XLB ¹⁰ _{2b/5b} P4D ⁰ P8B ² P16A ¹⁰	I/O	—	PD _S , R _U
	X0D17	XLB ⁰⁰ _{2b/5b} P4D ¹ P8B ³ P16A ¹¹	I/O	—	PD _S , R _U
	X0D18	XLB ⁰¹ _{2b/5b} P4D ² P8B ⁴ P16A ¹²	I/O	—	PD _S , R _U
	X0D19	XLB ¹¹ _{2b/5b} P4D ³ P8B ⁵ P16A ¹³	I/O	—	PD _S , R _U
	X0D20	XLB ²¹ _{3b} P4C ² P8B ⁶ P16A ¹⁴ P32A ³⁰	I/O	—	PD _S , R _U
	X0D21	XLB ³¹ _{5b} P4C ³ P8B ⁷ P16A ¹⁵ P32A ³¹	I/O	—	PD _S , R _U
	X0D22	XLB ⁴¹ _{5b} P1G ⁰	I/O	—	PD _S , R _U
	X0D23	P1H ⁰	I/O	—	PD _S , R _U
	X0D24	P1I ⁰	I/O	—	PD _S
	X0D25	P1J ⁰	I/O	—	PD _S
	X0D34	P1K ⁰	I/O	—	PD _S
	X0D35	P1L ⁰	I/O	—	PD _S
	X0D36	P1M ⁰ P8D ⁰ P16B ⁸	I/O	—	PD _S
	X0D37	P1N ⁰ P8D ¹ P16B ⁹	I/O	—	PD _S , R _U
	X0D38	P1O ⁰ P8D ² P16B ¹⁰	I/O	—	PD _S , R _U
	X0D39	P1P ⁰ P8D ³ P16B ¹¹	I/O	—	PD _S , R _U
	X0D52	XLC ¹⁰ _{2b} P32A ³	I/O	—	PD _S
	X0D53	XLC ⁰⁰ _{2b} P32A ⁴	I/O	—	PD _S
	X0D54	XLC ⁰¹ _{2b} P32A ⁵	I/O	—	PD _S
	X0D55	XLC ¹¹ _{2b} P32A ⁶	I/O	—	PD _S

4 Block Diagram



5 Product Overview

The XMOS XS1-L01A-TQ48 is a powerful device that provides a simple design process and highly-flexible solution to many applications. The device consists of a single xCORE Tile, which comprises a flexible multicore microcontroller with tightly integrated I/O and on-chip memory. The processor runs multiple tasks simultaneously using logical cores, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. Logical cores use channels to exchange data within a tile or across tiles. Multiple devices can be deployed and connected using an integrated switching network, enabling more resources to be added to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

The device can be configured using a set of software components that are rapidly customized and composed. XMOS provides source code libraries for many standard components. The device can be programmed using high-level languages such as C/C++ and XMOS-originated extensions to C, called XC, that simplify the control over concurrency, I/O and time.

The XMOS toolchain includes compilers, a simulator, debugger and static timing analyzer. The combination of real-time software, a compiler and timing analyzer enables the programmer to close timings on components of the design without a detailed understanding of the hardware characteristics.

5.1 Logical cores, Synchronizers and Locks

The xCORE Tile has up to eight active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for n cores). Figure 1 shows the guaranteed core performance depending on the number of cores used.

Figure 1:
Core performance

Speed Grade	Minimum MIPS per core (for n cores)							
	1	2	3	4	5	6	7	8
400 MHz	100	100	100	100	80	67	57	50
500 MHz	125	125	125	125	100	83	71	63

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum.

5.2 Channel Ends, Links and Switch

Logical cores communicate using point-to-point connections formed between two channel ends. Between tiles, channel communications are implemented over xConnect Links and routed through switches. The links operate in either 2bit/direction or 5bit/direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link. A total of four 5bit links are available between both cores.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, [X2999](#).

5.3 Ports and Clock Blocks

Ports provide an interface between the logical cores and I/O pins. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The operation of each port is synchronized to a clock block. A clock block can be connected to an external clock input, or it can be run from the divided reference clock. A clock block can also output its signal to a pin. On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

The ports and links are multiplexed, allowing the pins to be configured for use by ports of different widths or links. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

5.4 Timers

Timers are 32-bit counters that are relative to the xCORE Tile reference clock. A timer is defined to tick every 10 ns. This value is derived from the reference clock, which is configured to tick at 100 MHz by default.

5.5 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock. The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 2:

Figure 2 also lists the values of OD , F and R , which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

Figure 2:
PLL multiplier values and MODE pins

Oscillator Frequency	MODE		Tile Frequency	PLL Ratio	PLL settings		
	1	0			OD	F	R
5-13 MHz	0	0	130-399.75 MHz	30.75	1	122	0
13-20 MHz	1	1	260-400.00 MHz	20	2	119	0
20-48 MHz	1	0	167-400.00 MHz	8.33	2	49	0
48-100 MHz	0	1	196-400.00 MHz	4	2	23	0

OD, F and R must be chosen so that $0 \leq R \leq 63$, $0 \leq F \leq 4095$, $0 \leq OD \leq 7$, and $260MHz \leq F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \leq 1.3GHz$. The OD, F, and R values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value until the third rising edge of the system clock following the deassertion of the system reset.

For 500 MHz parts, once booted, the PLL must be reprogrammed to provide this tile frequency. The XMOS tools perform this operation by default.

Further details on configuring the clock can be found in the XS1-L Clock Frequency Control document, [X1433](#).

5.6 Boot ROM

The xCORE Tile boot procedure is illustrated in Figure 3. In normal usage, MODE[3:2] controls the boot source according to the table in Figure 4. If bit 5 of the security register (see §5.7.1) is set, the device boots from OTP.

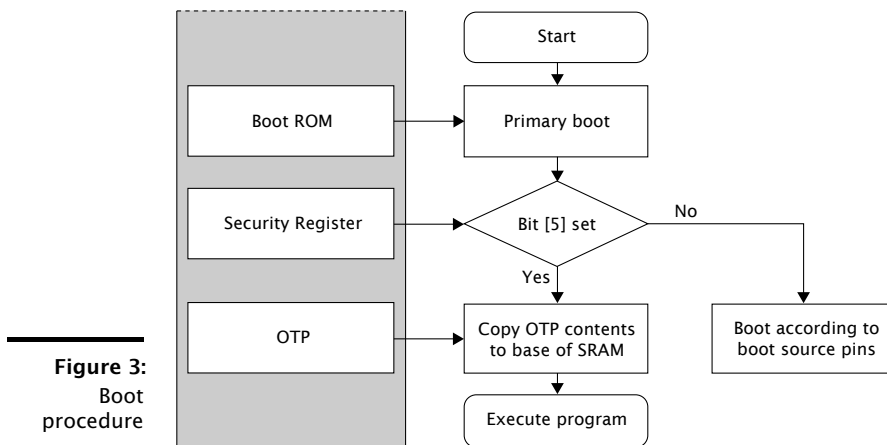


Figure 4:
Boot source pins

MODE[3]	MODE[2]	Boot Source		
0	0	None: Device waits to be booted via JTAG		
0	1	Reserved		
1	0	xConnect Link B		
1	1	SPI		
		Pin ^A	Signal	Description
		X0D00	MISO	Master In Slave Out (Data)
		X0D01	SS	Slave Select
		X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)		

^A The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. An SPI boot program can be burned into OTP and used at any time.

5.7 OTP

The xCORE Tile integrates 8KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in 2k rows x 32-bit configuration which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

5.7.1 Security Register

The security register enables the following security features:

- ▶ **Secure Boot:** The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (see §5.6). This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.
- ▶ **Disable JTAG:** The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
- ▶ **Disable Link access:** Other tiles are forbidden access to the processor state via the system switch.
Disabling both JTAG and Link access transforms an xCORE Tile into a “secure island” with other tiles free for non-secure user application code.
- ▶ **OTP Master and Sector Lock:** Further access to the OTP is prevented by setting the master lock. Locks can also be applied to each of the four OTP sectors individually.

These security features provide a strong level of protection and are sufficient for providing strong IP security.

5.8 SRAM

The xCORE Tile integrates a single 64 KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

5.9 JTAG

The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory.

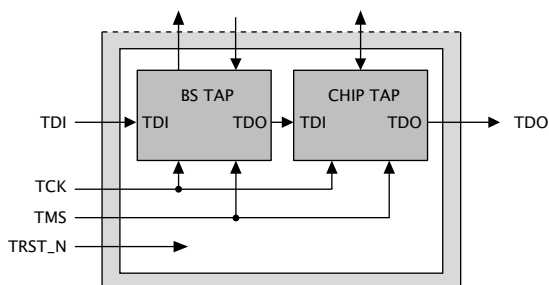


Figure 5:
JTAG chain structure

The JTAG chain structure is illustrated in Figure 5. Directly after reset, two TAP controllers are present in the JTAG chain: the boundary scan TAP and the chip TAP. The boundary scan TAP is a standard 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. The chip TAP provides access into the xCORE Tile, switch and OTP for loading code and debugging.

The TRST_N pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the TRST_N pin can be tied to ground to hold the JTAG module in reset.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 6.

Bit31	Device Identification Register												Bit0															
Version				Part Number								Manufacturer Identity						1										
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	1
0				0				0				2		6		3		3										

Figure 6:
IDCODE return value

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 7. The OTP User ID field is read from bits [22:31] of the security register (all zero on unprogrammed devices).

Figure 7:
USERCODE
return value

Usercode Register																																					
OTP User ID																						Unused				Silicon Revision											
Bit31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit0					
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
0						0						0				2				8				0				0				0					

5.10 Power Supplies

The device has the following types of power supply pins:

- ▶ VDD pins for the xCORE Tile tile
- ▶ VDDIO pins for the I/O lines
- ▶ PLL_AVDD pins for the PLL

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The VDDIO supply must ramp to its final value before VDD reaches 0.4 V.

The PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 Ω resistor and 100 nF multi-layer ceramic capacitor) is recommended on this pin.

The following ground pins are provided:

- ▶ GND for all supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (see §5.6). RST_N must be asserted low during and after power up for 100 ns.

6 DC and Switching Characteristics

6.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIO	I/O supply voltage	3.00	3.30	3.60	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	
Cl	xCORE Tile I/O load capacitance			25	pF	
Ta	Ambient operating temperature	0		70	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

Figure 8:
Operating conditions

6.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2.00		3.60	V	A
V(IL)	Input low voltage	-0.30		0.70	V	A
V(OH)	Output high voltage	2.70			V	B, C
V(OL)	Output low voltage			0.60	V	B, C
R(PU)	Pull-up resistance		35K		Ω	D
R(PD)	Pull-down resistance		35K		Ω	D

Figure 9:
DC characteristics

- A All pins except power supply pins.
- B Ports 1A, 1D, 1E, 1H, 1I, 1J, 1K and 1L are nominal 8 mA drivers, the remainder of the general-purpose I/Os are 4 mA.
- C Measured with 4 mA drivers sourcing 4 mA, 8 mA drivers sourcing 8 mA.
- D Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.

6.3 ESD Stress Voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model	-2.00		2.00	KV	
MM	Machine model	-200		200	V	

Figure 10:
ESD stress voltage

6.4 Reset Timing

Symbol	Parameters	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	5			μs	
T(INIT)	Initialization time			150	μs	A

- A Shows the time taken to start booting after RST_N has gone high.

6.5 Power Consumption

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		14		mA	A, B, C
PD	Tile power dissipation		450		μW/MIPS	A, D, E, F
IDD	Active VDD current (Speed Grade 4)		160	330	mA	A, G
	Active VDD current (Speed Grade 5)		200	330	mA	A, H
I(ADDPLL)	PLL_AVDD current			7	mA	I

Figure 12:
xCORE Tile currents

- A Use for budgetary purposes only.
- B Assumes typical tile and I/O voltages with no switching activity.
- C Includes PLL current.
- D Assumes typical tile and I/O voltages with nominal switching activity.
- E Assumes 1 MHz = 1 MIPS.
- F PD(TYP) value is the usage power consumption under typical operating conditions.
- G Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 400 MHz, average device resource usage.
- H Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.
- I PLL_AVDD = 1.0 V



The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.

More detailed power analysis can be found in the XS1-L Power Consumption document, [X2999](#).

6.6 Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	4.22	20	100	MHz	
SR	Slew rate	0.10			V/ns	
TJ(LT)	Long term jitter (pk-pk)			2	%	A
f(MAX)	Processor clock frequency (Speed Grade 4)			400	MHz	B
	Processor clock frequency (Speed Grade 5)			500	MHz	B

Figure 13:
Clock

- A Percentage of CLK period.
- B Assumes typical tile and I/O voltages with nominal activity.

Further details can be found in the XS1-L Clock Frequency Control document, [X1433](#).

6.7 xCORE Tile I/O AC Characteristics

Figure 14:
I/O AC characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, [X5821](#).

6.8 xConnect Link Performance

Figure 15:
Link performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	A, B
B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	B
B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	B

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

6.9 JTAG Timing

Figure 16:
JTAG timing

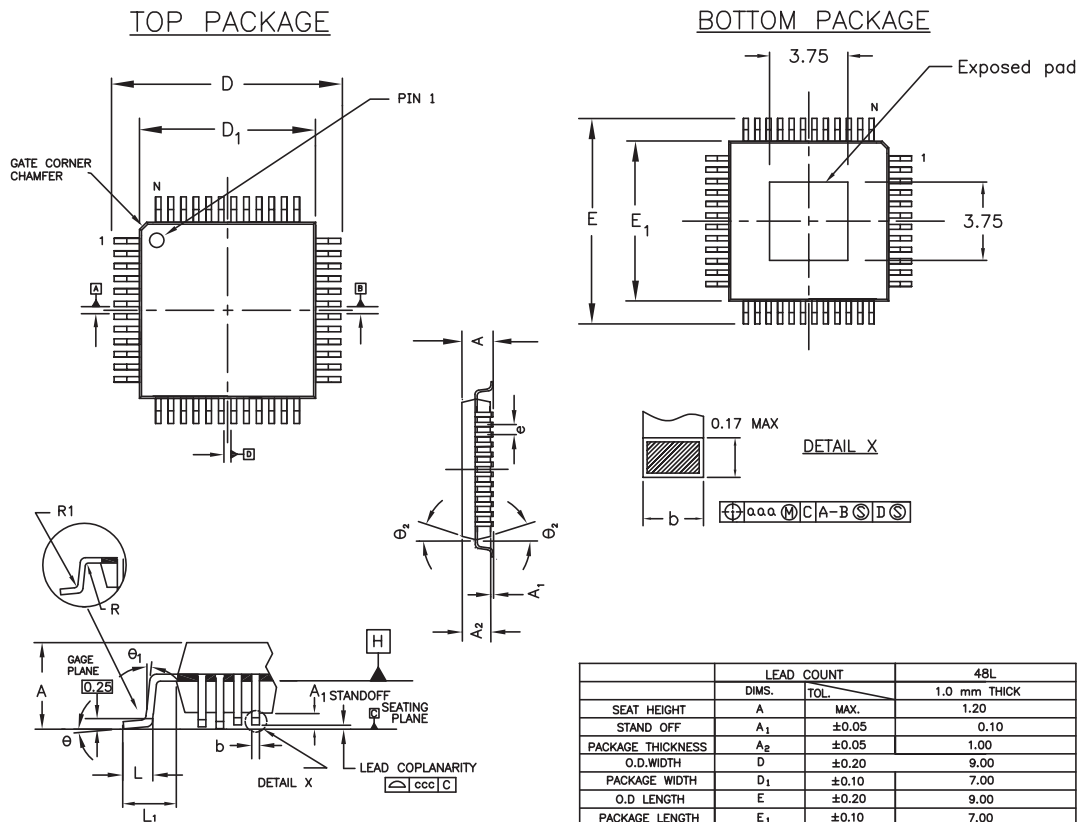
Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			18	MHz	
f(TCK_B)	TCK frequency (boundary scan)			10	MHz	
T(SETUP)	TDO to TCK setup time	5			ns	A
T(HOLD)	TDO to TCK hold time	5			ns	A
T(DELAY)	TCK to output delay			15	ns	B

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.

7 Package Information



NOTES:

1. All dimensions in millimeters.
2. Dimension tolerances shall be ± 0.05 mm unless otherwise specified.
3. Foot length 'L' is measured at gage plane 0.25mm above seating plane.
4. Dimension D1 and E1 are bottom package width and length and are measured at datum plane H.
5. Leadframe material: Eftec 64T Cu (or equivalent), 0.127mm (0.005") thick.

	LEAD COUNT		48L
	DIMS.	TOL.	1.0 mm THICK
SEAT HEIGHT	A	MAX.	1.20
STAND OFF	A ₁	± 0.05	0.10
PACKAGE THICKNESS	A ₂	± 0.05	1.00
O.D.WIDTH	D	± 0.20	9.00
PACKAGE WIDTH	D ₁	± 0.10	7.00
O.D LENGTH	E	± 0.20	9.00
PACKAGE LENGTH	E ₁	± 0.10	7.00
FOOT LENGTH	L	$+0.15/-0.10$	0.60
HALF FOOTPRINT	L ₁	REF	1.00
LEAD PITCH	e	TYPE	0.50
LEAD WIDTH	b	± 0.05	0.22
FOOT ANGLE	θ		0°-7°
VERTICAL ANGLE	θ_1		0° MIN.
	θ_2	$\pm 1^\circ$	12°
FIRST BEND	R	TYP	0.15
SECOND BEND	R ₁	± 0.05	0.15
	ggg	MAX.	0.08
COPLANARITY	ccc	MAX.	0.08
JEDEC REFERENCE DRAWING			MS-026
VARIATION DESIGNATOR			ABC

7.1 Part Marking

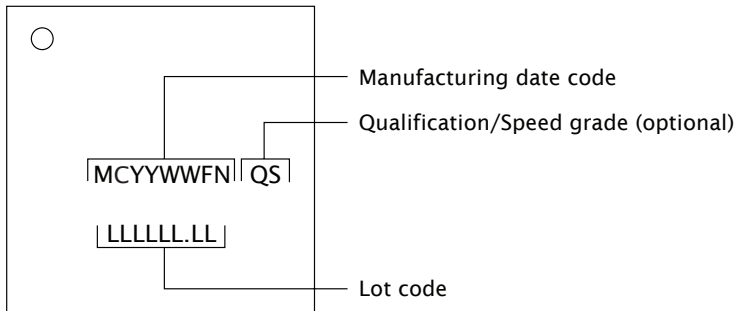


Figure 17:
Part marking scheme

8 Ordering Information

Figure 18:
Orderable part numbers

Product Code	Marking	Qualification	Speed Grade
XS1-L01A-TQ48-C4	MCYYWWL1	Commercial	400 MHz
XS1-L01A-TQ48-C5	MCYYWWL1 C5	Commercial	500 MHz
XS1-L01A-TQ48-C5-THS*	MCYYWWL1 TH5	Commercial	500 MHz

* MOQ and signed license agreement with XMOS required for access to Thesycon USB Audio Class 2.0 Production Driver (XS1-L1 Windows).

9 Development Tools

XMOS provides a comprehensive suite of development tools. Source files, timing scripts and a board design file are input to the compiler toolchain which produces a binary executable. This executable file can be simulated, loaded onto the device and debugged over JTAG, programmed into flash memory on the board or written to OTP memory on the device. The tools can also encrypt the flash image and write the decryption key securely to OTP memory.

The tools can be driven from either a graphical development environment or the command line and are supported on Windows, Linux and MacOS X. The tools are available at no cost from xmos.com/downloads. Information on using the tools is provided in a separate user guide, X1013.

10 Addendum: XMOS USB Interface

XMOS provides a low-level USB interface for connecting the device to a USB transceiver using the UTMI+ Low Pin Interface (ULPI). The ULPI signals must be connected to the pins named in Figure 19. Note also that some ports on the same tile are used internally and are not available for use when the USB driver is active (they are available otherwise).

Figure 19:
ULPI signals
provided by
the XMOS
USB driver

Pin	Signal
XnD12	ULPI_STEP
XnD13	ULPI_NXT
XnD14	ULPI_DATA[0]
XnD15	ULPI_DATA[1]
XnD16	ULPI_DATA[2]

Pin	Signal
XnD17	ULPI_DATA[3]
XnD18	ULPI_DATA[4]
XnD19	ULPI_DATA[5]
XnD20	ULPI_DATA[6]
XnD21	ULPI_DATA[7]

Pin	Signal
XnD22	ULPI_DIR
XnD23	ULPI_CLK
XnD37	Unavailable
XnD38	
XnD39	

11 Device Errata

This section describes minor operational differences from the data sheet and recommended workarounds. As device and documentation issues become known, this section will be updated the document revised.

To guarantee a logic low is seen on the pins RST_N, MODE[3:0], TRST_N, TMS, TCK and TDI, the driving circuit should present an impedance of less than 100Ω to ground. Usually this is not a problem for CMOS drivers driving single inputs. If one or more of these inputs are placed in parallel, however, additional logic buffers may be required to guarantee correct operation.

For static inputs tied high or low, the relevant input pin should be tied directly to GND or VDDIO.

12 Associated Design Documentation

Document Title	Information	Document Number
XS1-L Hardware Design Checklist	Board design checklist	X6277
Device Package User Guide	Land pattern, solder paste, ground recommendations	X4979
Estimating Power Consumption For XS1-L Devices	Power consumption	X4271
Programming XC on XMOS Devices	Timers, ports, clocks, cores and channels	X9577
XMOS Tools User Guide	Compilers, assembler and linker/mapper Timing analyzer and debugger Flash and OTP programming utilities	X1013

- ▶ Example schematic diagrams detailing minimal system configurations are available from <http://www.xmos.com/support/silicon>.

13 Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	X7879
XS1 Port I/O Timing	Port timings	X5821
XS1-L System Specification	Link, switch and system information	X2725
XS1-L Link Performance and Design Guidelines	Link timings	X2999
XS1-L Clock Frequency Control	Advanced clock control	X1433
XS1-L Active Power Conservation	Low-power mode during idle	X5512

14 Revision History

The page numbers in this section refer to this document.

Rev. X8338F-10/12

1. Renamed XCore to xCORE Tile, and Thread to Core.
2. Instruction description updated - page 2.
3. Updated PL section - page 7.

Rev. X8338E-05/12-B

1. Block diagram updated: pins listed sequentially, 4-bit ports updated - page 5.

Rev. X8338D-05/12

1. Input voltage use for 1-bit ports updated footnote on page 12.
2. Pull up/down information updated for JTAG/MODE pins on page 4.
3. Updated use of TRST_N on page 10.
4. Clarified tables of pins used by USB Interface on page 16.
5. OTP section updated and moved before SRAM on page 10.

Rev. X8338C-03/12

1. Removed "Volatile" from Memory description on page 2.
2. Updated 32-bit port connection in block diagram on page 5.

Rev. X8338B-05/11

1. Removed references to DEBUG_N.
2. Updated Pin 40 to VDDIO in Pin Configuration on page 3
3. Changed XMOS Link references to XLA format in Signal Description on page 4.

Rev. X8338A-04/11

1. Initial release.



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