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Kind regards,

Team Nexperia

# PSMN3R4-30PL

N-channel 30 V 3.4 mΩ logic level MOSFET

Rev. 01 — 2 November 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in TO220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

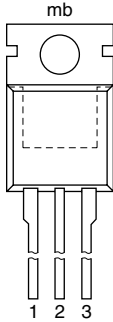
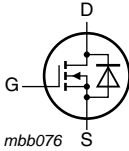
| Symbol                         | Parameter                                    | Conditions  | Min                | Typ | Max | Unit |
|--------------------------------|--|---|--------------------|-----|-----|------|
| $V_{DS}$                       | drain-source voltage                         | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$   | -                  | -   | 30  | V    |
| $I_D$                          | drain current                                | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$<br>see <a href="#">Figure 1</a>  | <a href="#">11</a> | -   | 100 | A    |
| $P_{tot}$                      | total power dissipation                      | $T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>   | -                  | -   | 114 | W    |
| $T_j$                          | junction temperature                         |   | -55                | -   | 175 | °C   |
| <b>Static characteristics</b>  |  |   |                    |     |     |      |
| $R_{DS(on)}$                   | drain-source on-state resistance             | $V_{GS} = 4.5\text{ V}; I_D = 10\text{ A};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 13</a>  | -                  | 3.5 | 4.1 | mΩ   |
|                                |  | $V_{GS} = 10\text{ V}; I_D = 10\text{ A};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 13</a>   | <a href="#">12</a> | -   | 2.8 | 3.4  |
| <b>Dynamic characteristics</b> |  |   |                    |     |     |      |
| $Q_{GD}$                       | gate-drain charge                            | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A};$<br>$V_{DS} = 15\text{ V};$ see <a href="#">Figure 14</a> ;                                      | -                  | 8   | -   | nC   |
| $Q_{G(tot)}$                   | total gate charge                            | see <a href="#">Figure 15</a>   | -                  | 31  | -   | nC   |
| <b>Avalanche ruggedness</b>    |  |   |                    |     |     |      |
| $E_{DS(AL)S}$                  | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$<br>$I_D = 100\text{ A}; V_{sup} \leq 30\text{ V};$<br>$R_{GS} = 50\text{ Ω};$ unclamped | -                  | -   | 200 | mJ   |



- [1] Continuous current is limited by package.
- [2] Measured 3 mm from package.

## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline  | Graphic symbol  |
|-----|--------|-----------------------------------|---|---|
| 1   | G      | gate                              |  |  |
| 2   | D      | drain                             |   |   |
| 3   | S      | source                            |   |   |
| mb  | D      | mounting base; connected to drain |   |   |

**SOT78 (TO-220AB)**

## 3. Ordering information

Table 3. Ordering information

| Type number  | Package  |  |         |
|--------------|----------|--|---------|
|              | Name     | Description  | Version |
| PSMN3R4-30PL | TO-220AB | plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB | SOT78   |

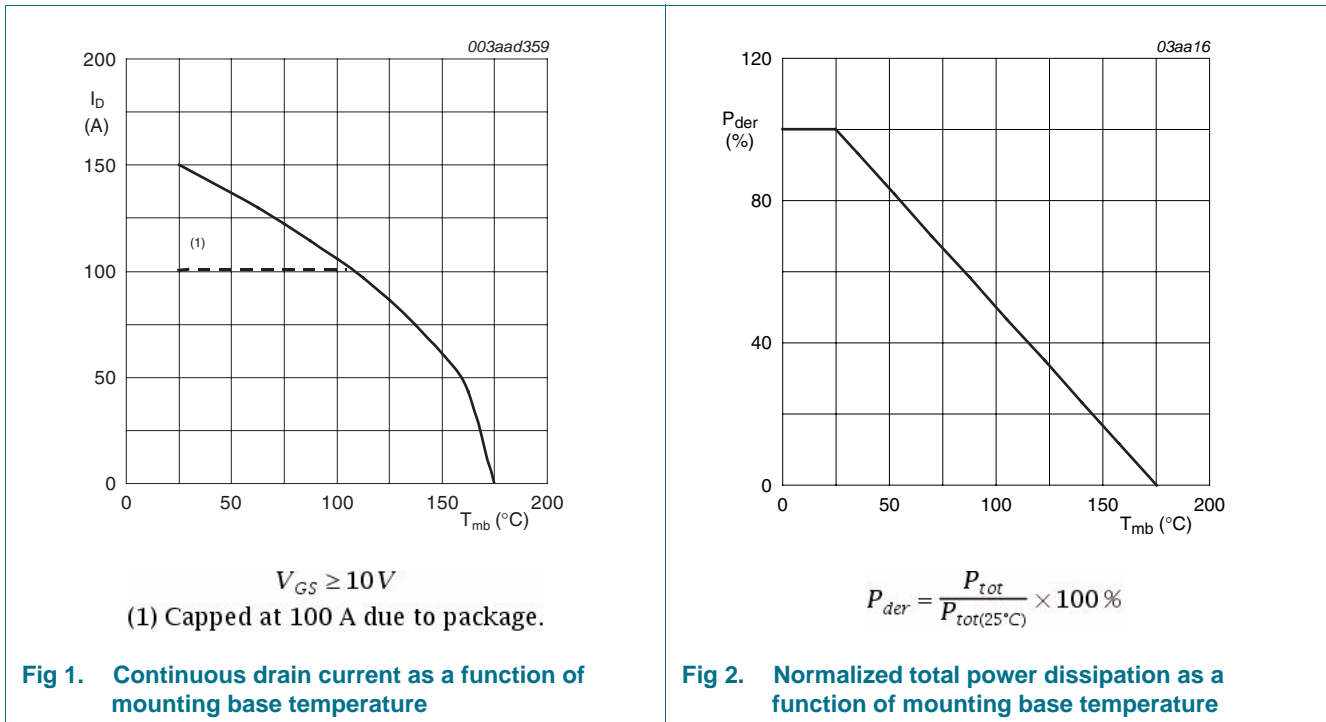
### 4. Limiting values

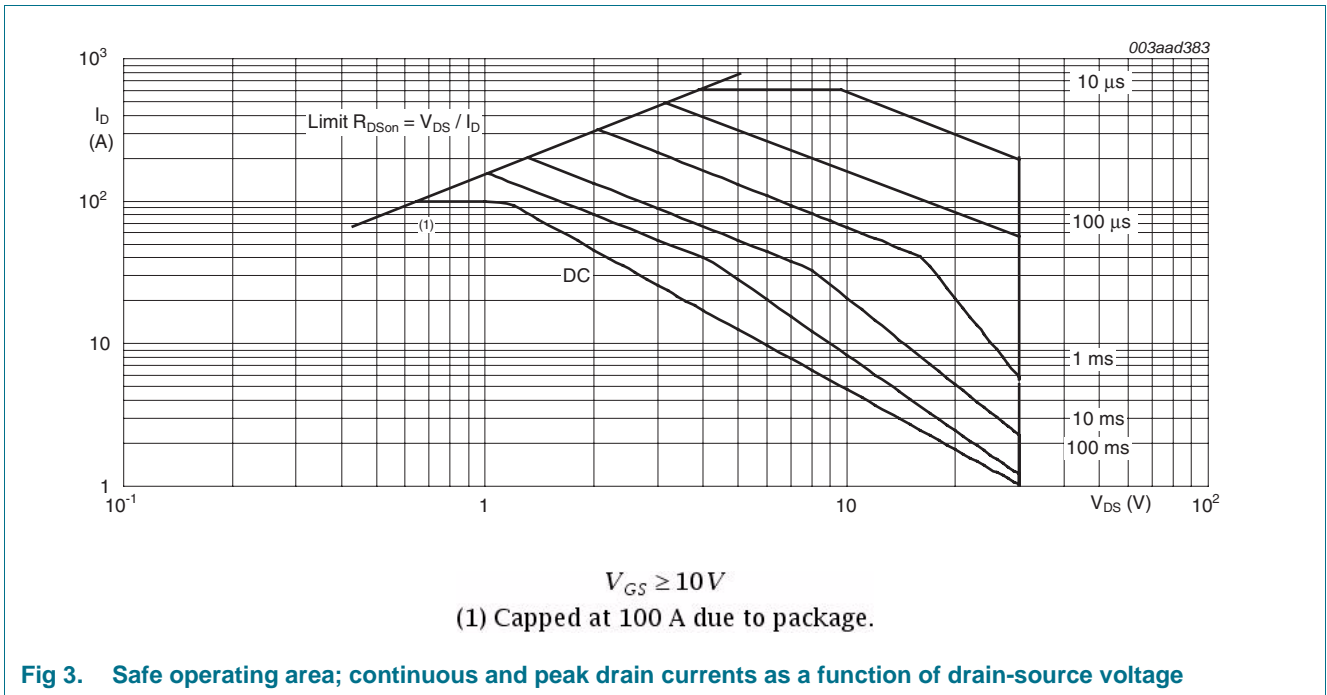
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions  | Min | Max | Unit |
|-----------------------------|--|---|-----|-----|------|
| V <sub>DS</sub>             | drain-source voltage                         | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C   | -   | 30  | V    |
| V <sub>DGR</sub>            | drain-gate voltage                           | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ  | -   | 30  | V    |
| V <sub>GS</sub>             | gate-source voltage                          |   | -20 | 20  | V    |
| I <sub>D</sub>              | drain current                                | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>  | [1] | 100 | A    |
|                             |  | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a>   | [1] | 100 | A    |
| I <sub>DM</sub>             | peak drain current                           | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>   | -   | 609 | A    |
| P <sub>tot</sub>            | total power dissipation                      | T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>   | -   | 114 | W    |
| T <sub>stg</sub>            | storage temperature                          |   | -55 | 175 | °C   |
| T <sub>j</sub>              | junction temperature                         |   | -55 | 175 | °C   |
| <b>Source-drain diode</b>   |  |   |     |     |      |
| I <sub>S</sub>              | source current                               | T <sub>mb</sub> = 25 °C   | [1] | 100 | A    |
| I <sub>SM</sub>             | peak source current                          | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C   | -   | 609 | A    |
| <b>Avalanche ruggedness</b> |  |   |     |     |      |
| E <sub>DS(AL)S</sub>        | non-repetitive drain-source avalanche energy | V <sub>GS</sub> = 10 V; T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped | -   | 200 | mJ   |

[1] Continuous current is limited by package.

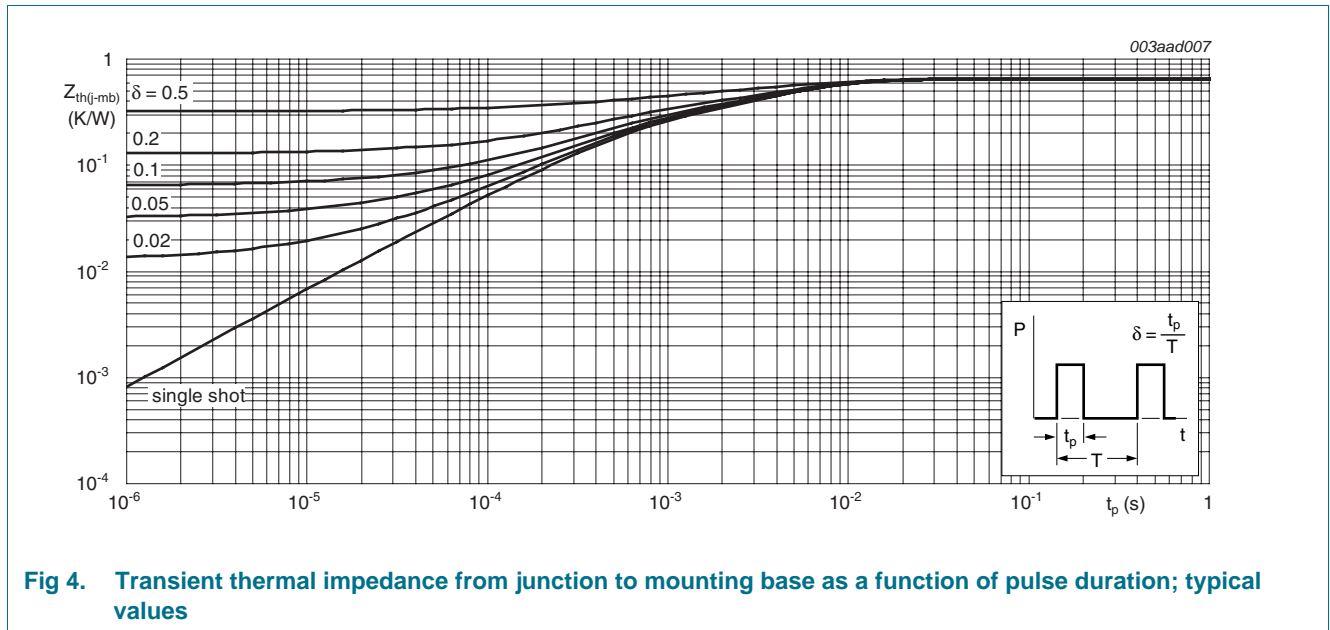




### 5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter   | Conditions                   | Min | Typ  | Max | Unit |
|----------------|---|------------------------------|-----|------|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 4</a> | -   | 0.65 | 1   | K/W  |



## 6. Characteristics

**Table 6. Characteristics**

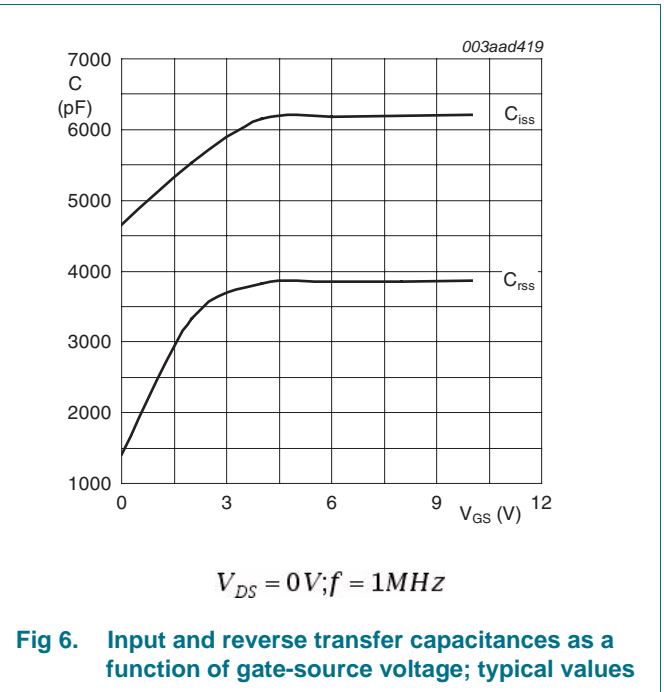
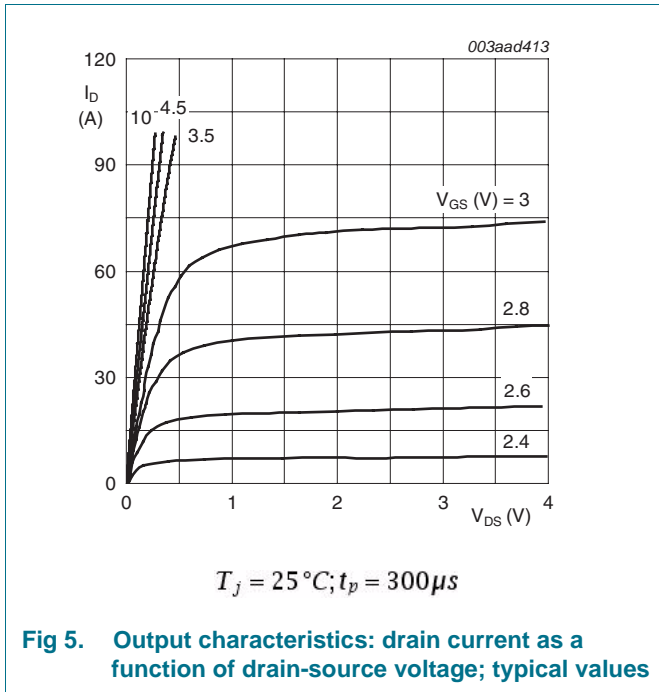
Tested to JEDEC standards where applicable.

| Symbol                         | Parameter                         | Conditions   | Min                | Typ  | Max  | Unit    |
|--------------------------------|-----------------------------------|--|--------------------|------|------|---------|
| <b>Static characteristics</b>  |                                   |  |                    |      |      |         |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage    | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$   | 30                 | -    | -    | V       |
|                                |                                   | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$  | 27                 | -    | -    | V       |
| $V_{GS(th)}$                   | gate-source threshold voltage     | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a> | 1.3                | 1.7  | 2.15 | V       |
|                                |                                   | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>                                | 0.5                | -    | -    | V       |
|                                |                                   | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>                                | -                  | -    | 2.45 | V       |
| $I_{DSS}$                      | drain leakage current             | $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$   | -                  | 0.3  | 5    | $\mu A$ |
|                                |                                   | $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$  | -                  | -    | 100  | $\mu A$ |
| $I_{GSS}$                      | gate leakage current              | $V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$   | -                  | 10   | 100  | nA      |
|                                |                                   | $V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$  | -                  | 10   | 100  | nA      |
| $R_{DS(on)}$                   | drain-source on-state resistance  | $V_{GS} = 10 V; I_D = 10 A; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>  | -                  | -    | 6.46 | mΩ      |
|                                |                                   | $V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>  | -                  | 3.5  | 4.1  | mΩ      |
|                                |                                   | $V_{GS} = 10 V; I_D = 10 A; T_j = 100 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>  | -                  | -    | 6.1  | mΩ      |
|                                |                                   | $V_{GS} = 4.5 V; I_D = 10 A; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>   | -                  | -    | 7.79 | mΩ      |
|                                |                                   | $V_{GS} = 10 V; I_D = 10 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>   | <a href="#">11</a> | -    | 2.8  | 3.4     |
| $R_G$                          | gate resistance                   | $f = 1 \text{ MHz}$  | -                  | 1    | -    | Ω       |
| <b>Dynamic characteristics</b> |                                   |  |                    |      |      |         |
| $Q_{G(tot)}$                   | total gate charge                 | $I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                       | -                  | 64   | -    | nC      |
|                                |                                   | $I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$   | -                  | 58   | -    | nC      |
|                                |                                   | $I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                      | -                  | 31   | -    | nC      |
| $Q_{GS}$                       | gate-source charge                |  | -                  | 12   | -    | nC      |
| $Q_{GS(th)}$                   | pre-threshold gate-source charge  |  | -                  | 6.2  | -    | nC      |
| $Q_{GS(th-pl)}$                | post-threshold gate-source charge |  | -                  | 5.8  | -    | nC      |
| $Q_{GD}$                       | gate-drain charge                 |  | -                  | 8    | -    | nC      |
| $V_{GS(pl)}$                   | gate-source plateau voltage       | $V_{DS} = 15 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>  | -                  | 2.8  | -    | V       |
| $C_{iss}$                      | input capacitance                 | $V_{DS} = 12 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ;   | -                  | 3907 | -    | pF      |
| $C_{oss}$                      | output capacitance                | $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 16</a>  | -                  | 822  | -    | pF      |
| $C_{rss}$                      | reverse transfer capacitance      |  | -                  | 356  | -    | pF      |

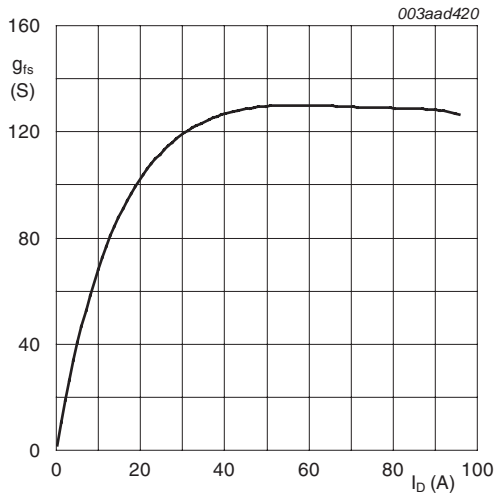
**Table 6. Characteristics ...continued**  
 Tested to JEDEC standards where applicable.

| Symbol                    | Parameter             | Conditions   | Min | Typ | Max | Unit |
|---------------------------|-----------------------|--|-----|-----|-----|------|
| $t_{d(on)}$               | turn-on delay time    | $V_{DS} = 12\text{ V}; R_L = 0.5\ \Omega;$   | -   | 40  | -   | ns   |
| $t_r$                     | rise time             | $V_{GS} = 4.5\text{ V}; R_{G(ext)} = 4.7\ \Omega$  | -   | 73  | -   | ns   |
| $t_{d(off)}$              | turn-off delay time   |  | -   | 59  | -   | ns   |
| $t_f$                     | fall time             |  | -   | 28  | -   | ns   |
| <b>Source-drain diode</b> |                       |  |     |     |     |      |
| $V_{SD}$                  | source-drain voltage  | $I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$<br>see <a href="#">Figure 17</a> | -   | 0.7 | 1.2 | V    |
| $t_{rr}$                  | reverse recovery time | $I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s};$  | -   | 36  | -   | ns   |
| $Q_r$                     | recovered charge      | $V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}$  | -   | 28  | -   | nC   |

[1] Measured 3 mm from package.

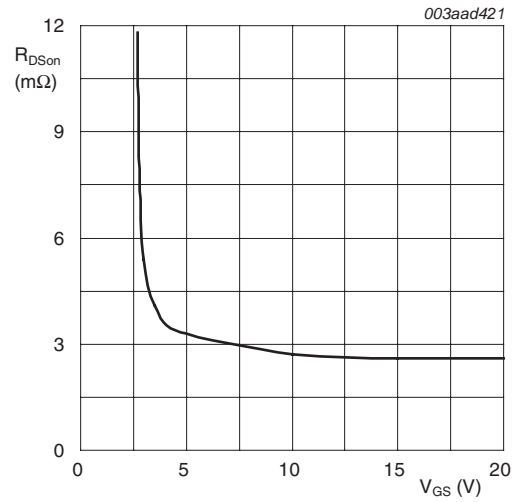






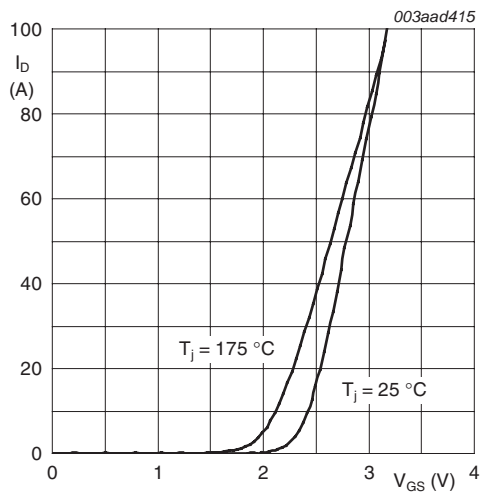
$T_j = 25^\circ\text{C}; V_{DS} = 15\text{V}$

Fig 7. Forward transconductance as a function of drain current; typical values



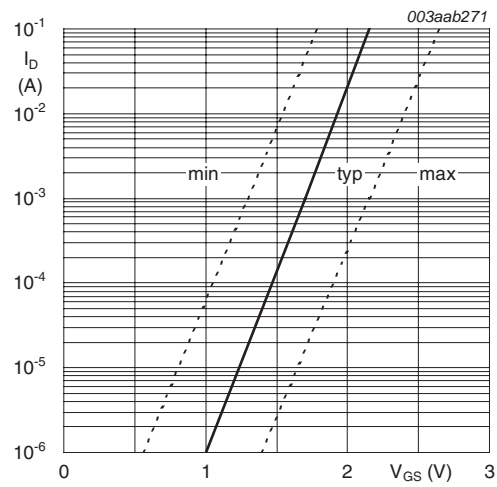
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



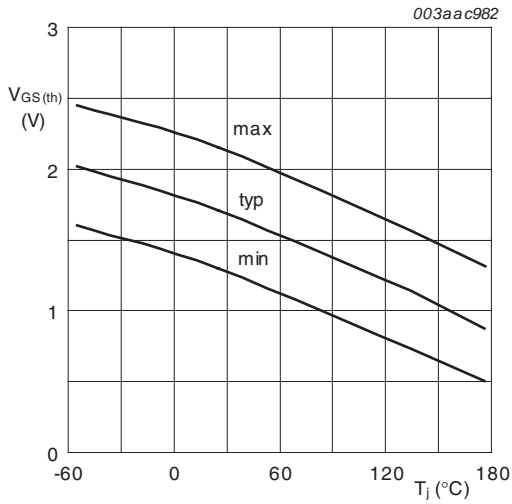
$V_{DS} = 15\text{V}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



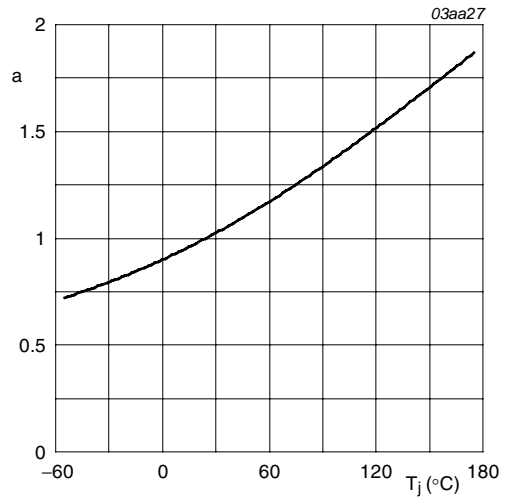
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



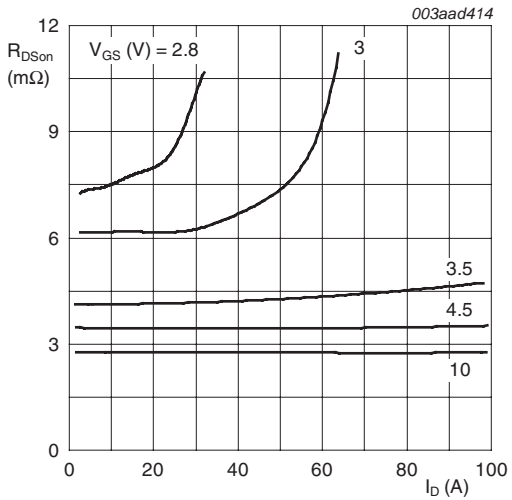
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25^\circ\text{C}; t_p = 300\ \mu\text{s}$$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

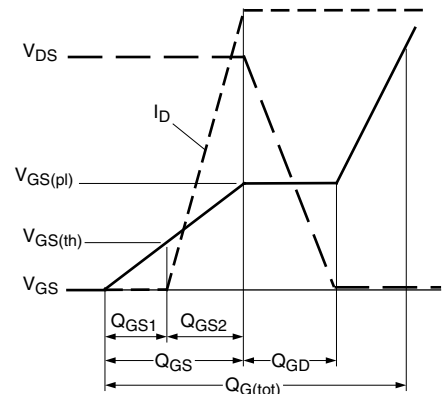
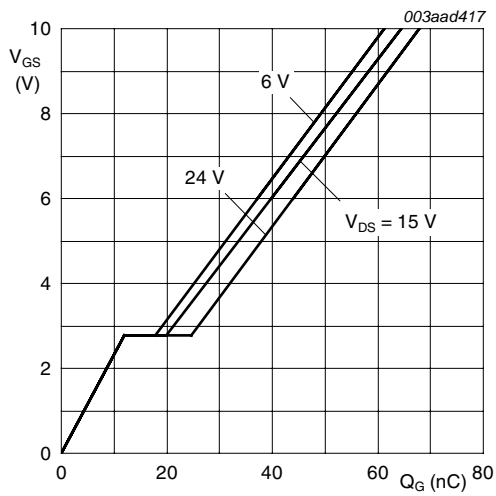
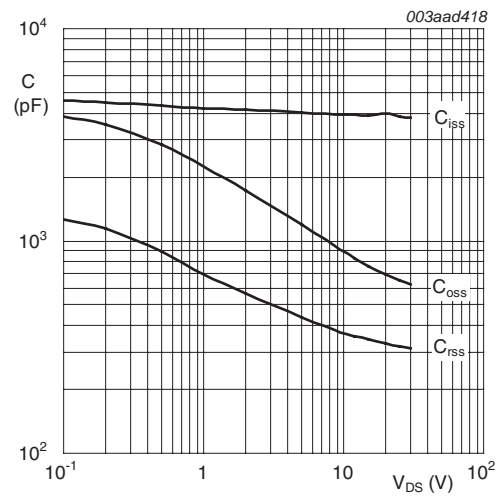


Fig 14. Gate charge waveform definitions



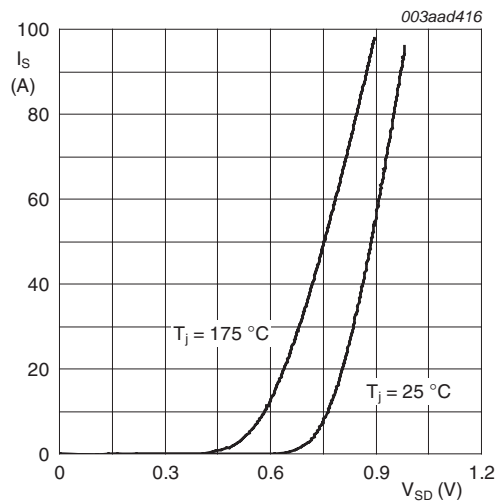
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

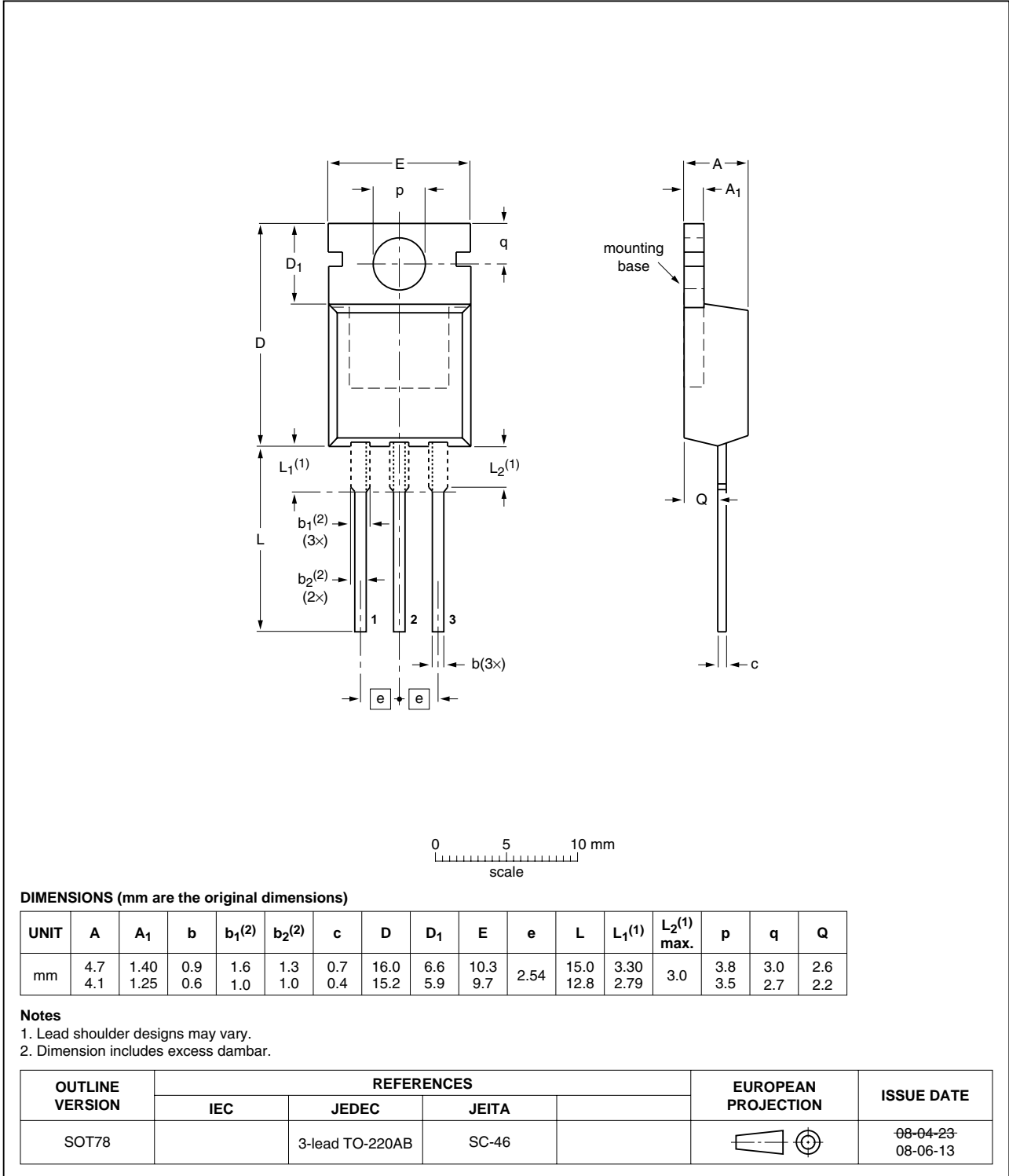


Fig 18. Package outline SOT78 (TO-220AB)

## 8. Revision history

Table 7. Revision history

| Document ID      | Release date | Data sheet status  | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PSMN3R4-30PL v.1 | 20101102     | Product data sheet | -             | -          |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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