Si53159

PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 Nine Output Fanout Buffer

Features

- PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 common clock compliant
- Supports Serial-ATA (SATA) at 100 MHz
- Low power push-pull differential output buffers
- No termination resistors required
- Output enable pins for all buffered clocks
- Up to nine buffered clocks
- 100 to 210 MHz clock input range
- I^2C support with readback capabilities
- Supports spread spectrum input
- Extended temperature: –40 to 85 °C
- 3.3 V power supply
- 48-pin QFN package

Ordering Information:
See page 18.

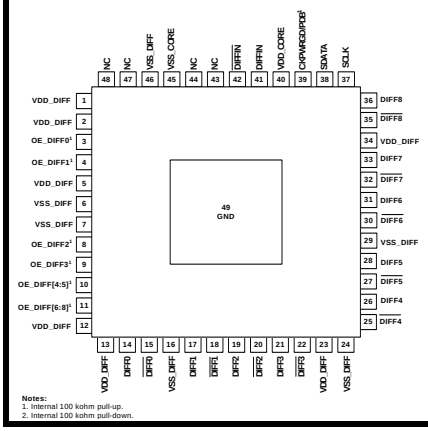
Applications

- Network attached storage
- Multi-function printers
- Wireless access point
- Servers

Description

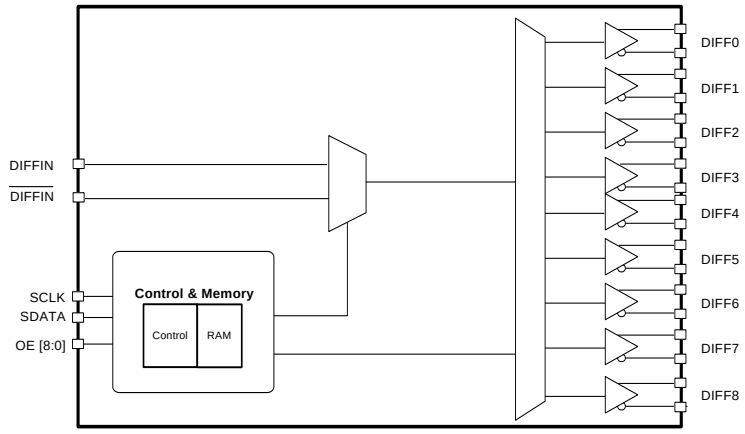
The Si53159 is a high-performance, low additive jitter, PCIe clock buffer that can fan out nine PCIe clocks. The clock outputs are compliant to PCIe Gen 1, Gen 2, Gen 3, and Gen 4 specifications. The device has six hardware output enable control pins for enabling and disabling differential outputs. The small footprint and low power consumption makes the Si53159 the ideal clock solution for consumer and embedded applications. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

Pin Assignments



Patents pending

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Operating Voltage	VDD core	3.3 ± 5%	3.135	—	3.465	V
3.3 V Input High Voltage	V_{IH}	Control input pins	2.0	—	V_{DD} + 0.3	V
3.3 V Input Low Voltage	V_{IL}	Control input pins	V_{SS} – 0.3	—	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	—	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	1.0	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	—	5	µA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	—	µA
High-impedance Output Current	I_{OZ}		–10	—	10	µA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	L_{IN}		—	—	7	nH
Power Down Current	I_{DD_PD}		—	—	1	mA
Dynamic Supply Current in Fanout Mode	$I_{DD\_3.3V}$	All outputs enabled, 5” traces; 2 pF load, frequency at 100 MHz	—	—	60	mA

Table 2. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DIFFIN at 0.7 V						
DIFFIN and $\overline{\text{DIFFIN}}$ Rising/Falling Slew Rate	T_R / T_F	Single ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525 V (Averaged)	0.6	—	4	V/ns
Differential Input High Voltage	V_{IH}		150	—	—	mV
Differential Input Low Voltage	V_{IL}		—	—	–150	mV
Crossing Point Voltage at 0.7 V Swing	V_{OX}	Single-ended measurement	250	—	550	mV
Vcross Variation Over All edges	ΔV_{OX}	Single-ended measurement	—	—	140	mV
Differential Ringback Voltage	V_{RB}		–100	—	100	mV
Time before Ringback Allowed	T_{STABLE}		500	—	—	ps
Absolute Maximum Input Voltage	V_{MAX}			—	1.15	V
Absolute Minimum Input Voltage	V_{MIN}		–0.3	—	—	V
DIFFIN and $\overline{\text{DIFFIN}}$ Duty Cycle	T_{DC}	Measured at crossing point V_{OX}	45	—	55	%
Rise/Fall Matching	T_{RFM}	Determined as a fraction of $2 \times (T_R - T_F)/(T_R + T_F)$	—	—	20	%
DIFF at 0.7 V						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Clock Skew	T_{SKEW}	Measured at 0 V differential	—	—	50	ps
PCIe Gen1 Pk-Pk Jitter	Pk-Pk	PCIe Gen 1	0	—	10	ps
PCIe Gen 2 Phase Jitter	RMS_{GEN2}	10 kHz < F < 1.5 MHz	0	—	0.5	ps
		1.5 MHz < F < Nyquist	0	—	0.5	ps
PCIe Gen 3 Phase Jitter	RMS_{GEN3}	Includes PLL BW 2–4 MHz, CDR = 10 MHz	0	—	0.10	ps
Additive PCIe Gen 4 Phase Jitter	RMS_{GEN4}	PCIe Gen 4	—	—	0.10	ps
Additive Cycle to Cycle Jitter	T_{CCJ}	In buffer mode. Measured at 0 V differential	—	20	50	ps
Long-term Accuracy	L_{ACC}	Measured at 0 V differential	—	—	100	ppm
Rising/Falling Slew rate	T_R / T_F	Measured differentially from ±150 mV	2.5	—	8	V/ns
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 2. AC Electrical Specifications (Continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Enable/Disable and Setup						
Clock Stabilization from Power-Up	T_{STABLE}	Measured from the point when both V_{DD} and clock input are valid	—	—	1.8	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 3. Absolute Maximum Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	4.6	V_{DC}
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Extended Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	—	22	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	—	30	°C/W
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)	V–0			

Note: **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

2. Functional Description

2.1. CKPWRGD/PDB (Power Down) Pin

The CKPWRGD/PDB pin is a dual-function pin. During initial power up, the pin functions as the CKPWRGD pin. Upon the first power up, if the CKPWRGD pin is low, the outputs will be disabled, but the crystal oscillator and I^2C logic will be active. Once the CKPWRGD pin has been sampled high by the clock chip, the pin assumes a PDB functionality. When the pin has assumed a PDB functionality and is pulled low, the device will be placed in power down mode. The CKPWRGD/PDB pin is required to be driven at all times even though it has an internal 100 kΩ resistor.

2.2. PDB (Power Down) Assertion

The PDB pin is an asynchronous active low input used to disable all output clocks in a glitch-free manner. All outputs will be driven low in power down mode. In power down mode, all outputs, the crystal oscillator, and the I^2C logic are disabled.

2.3. PDB Deassertion

When a valid rising edge on CKPWRGD/PDB pin is applied, all outputs are enabled in a glitch-free manner within two to six output clock cycles.

2.4. OE Pin

The OE pin is an active high input used to enable and disable the output clock. To enable the output clock, the OE pin and the I^2C OE bit need to be a logic high. By default, the OE pin and the I^2C OE bit are set to a logic high. There are two methods to disable the output clock: the OE pin is pulled to a logic low, or the I^2C OE bit is set to a logic low. The OE pin is required to be driven at all times even though it has an internal 100 kΩ resistor.

2.5. OE Assertion

The OE pin is an active high input used for synchronous stopping and starting the respective output clock while the rest of the clock generator continues to function. The assertion of the OE function is achieved by pulling the OE pin and the I^2C OE bit high which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

2.6. OE Deassertion

The OE function is deasserted by pulling the pin or the I^2C OE bit to a logic low. The corresponding output is stopped cleanly and the final output state is driven low.

3. Test and Measurement Setup

This diagram shows the test load configuration for the differential clock signals.

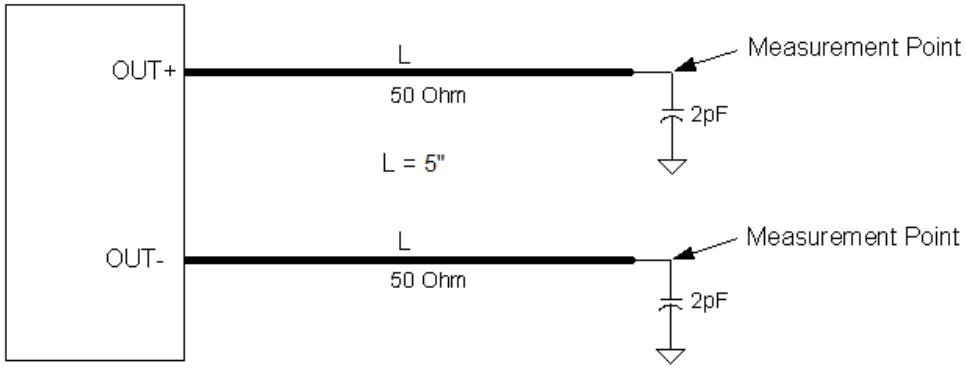


Figure 1. 0.7 V Differential Load Configuration

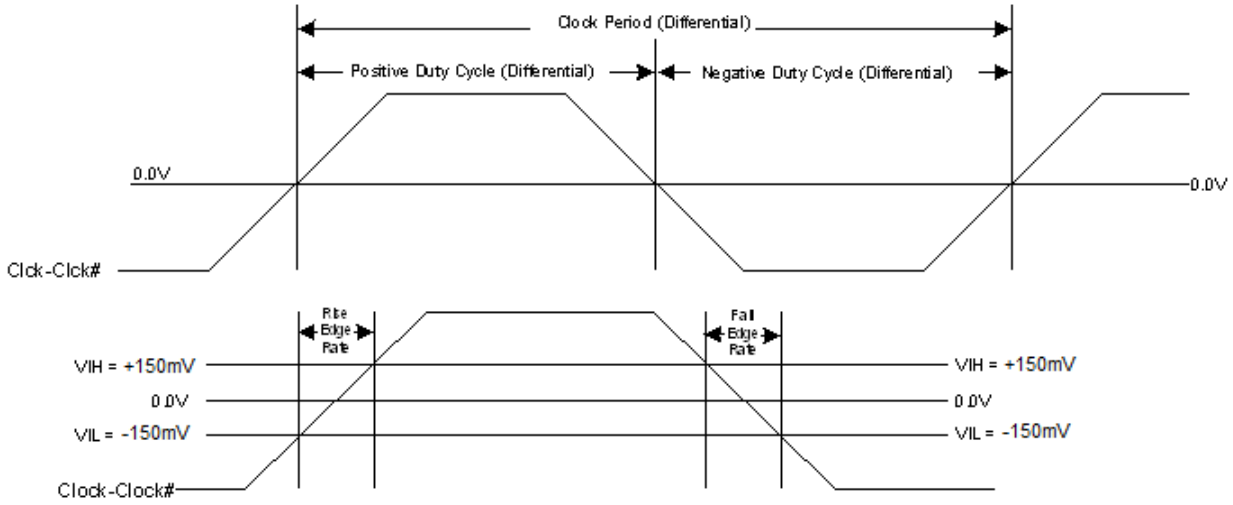


Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

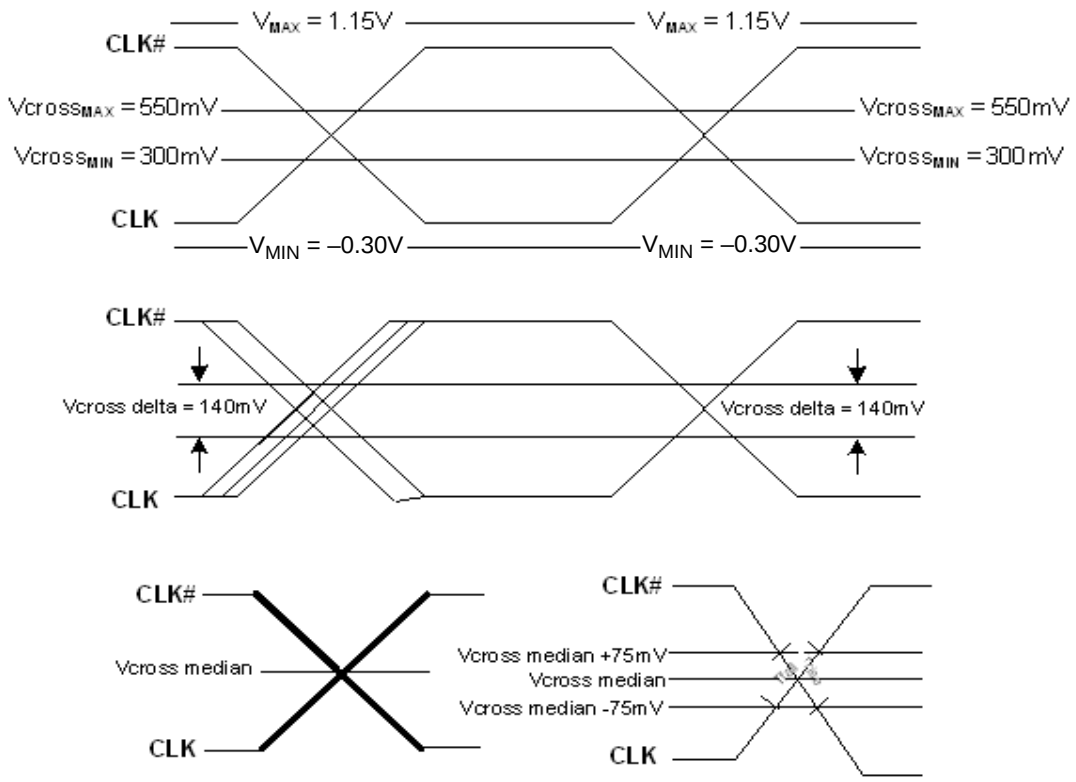


Figure 3. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Control Registers

4.1. I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. Through the I²C interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the I²C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

4.2. Data Protocol

The clock driver I²C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 4 on page 10 while Table 5 on page 11 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address—7 bits	8:2	Slave address—7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code—8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count—8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address—7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave—8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave—8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave—8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave—8 bits
		....	NOT Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000000

Bit	Name	Function
7:0	Reserved	

Control Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DIFF0_OE		DIFF1_OE	DIFF2_OE	DIFF3_OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00010111

Bit	Name	Function
7:5	Reserved	
4	DIFF0_OE	**Output Enable for DIFF0.** 0: Output disabled. 1: Output enabled.
3	Reserved	
2	DIFF1_OE	**Output Enable for DIFF1.** 0: Output disabled. 1: Output enabled.
1	DIFF2_OE	**Output Enable for DIFF2.** 0: Output disabled. 1: Output enabled.
0	DIFF3_OE	**Output Enable for DIFF3.** 0: Output disabled. 1: Output enabled.

Control Register 2. Byte 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF4_OE	DIFF5_OE	DIFF6_OE	DIFF7_OE	DIFF8_OE			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11111000

Bit	Name	Function
7	DIFF4_OE	**Output Enable for DIFF4.** 0: Output disabled. 1: Output enabled.
6	DIFF5_OE	**Output Enable for DIFF5.** 0: Output disabled. 1: Output enabled.
5	DIFF6_OE	**Output Enable for DIFF6.** 0: Output disabled. 1: Output enabled.
4	DIFF7_OE	**Output Enable for DIFF7.** 0: Output disabled. 1: Output enabled.
3	DIFF8_OE	**Output Enable for DIFF8.** 0: Output disabled. 1: Output enabled.
2:0	Reserved	

Control Register 3. Byte 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Rev Code[3:0]				Vendor ID[3:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001000

Bit	Name	Function
7:4	Rev Code[3:0]	**Program Revision Code.**
3:0	Vendor ID[3:0]	**Vendor Identification Code.**

Control Register 4. Byte 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000110

Bit	Name	Function
7:0	BC[7:0]	**Byte Count Register.**

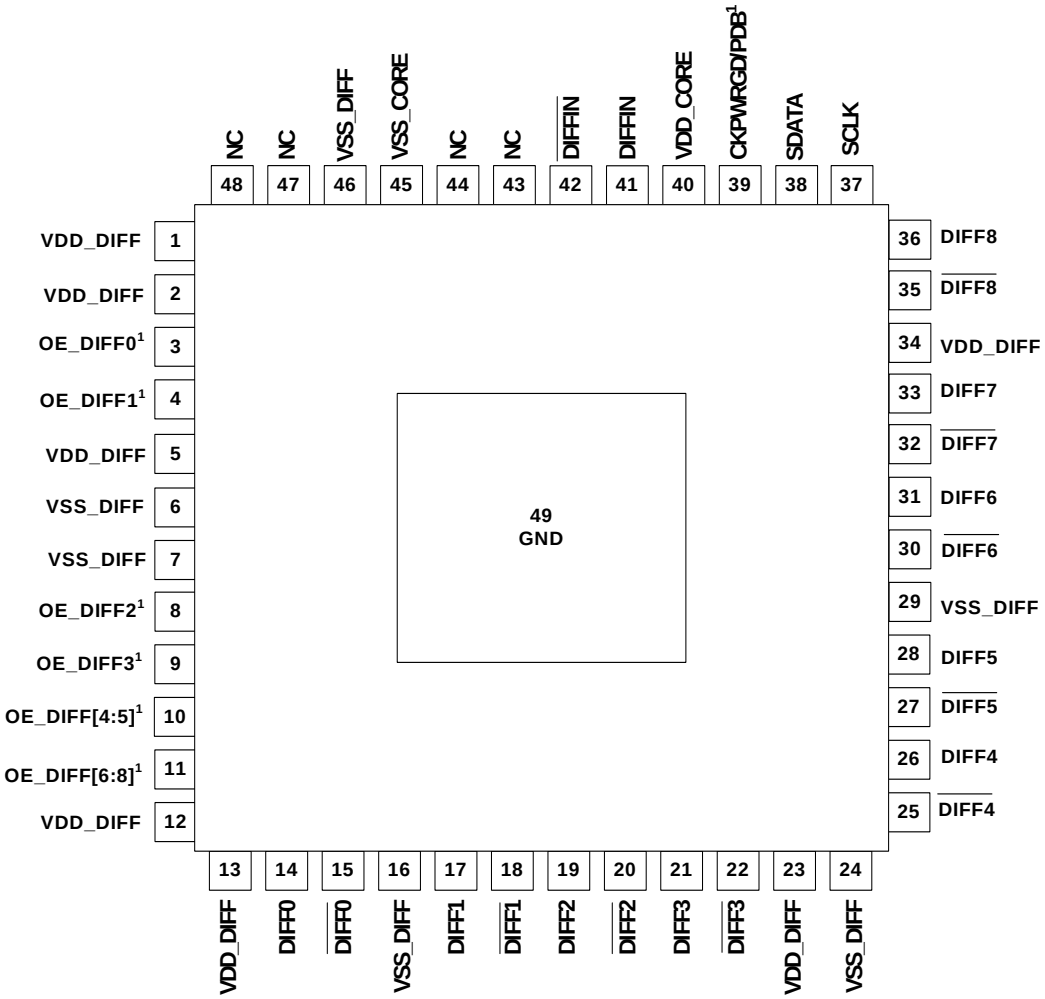
Control Register 5. Byte 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_Amp_Sel	DIFF_Amp_Cntl[2]	DIFF_Amp_Cntl[1]	DIFF_Amp_Cntl[0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11011000

Bit	Name	Function
7	DIFF_Amp_Sel	**Amplitude Control for DIFF Differential Outputs.** 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4].
6	DIFF_Amp_Cntl[2]	**DIFF Differential Outputs Amplitude Adjustment.** 000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV 100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV
5	DIFF_Amp_Cntl[1]	
4	DIFF_Amp_Cntl[0]	
3:0	Reserved	

5. Pin Descriptions: 48-Pin QFN



Notes:
1. Internal 100 kohm pull-up.
2. Internal 100 kohm pull-down.

Table 6. Si53159 48-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDD_DIFF	PWR	3.3 V power supply.
2	VDD_DIFF	PWR	3.3 V power supply.
3	OE_DIFF0	I,PU	Active high input pin enables DIFF0 (internal 100 kΩ pull-up).
4	OE_DIFF1	I,PU	Active high input pin enables DIFF1 (internal 100 kΩ pull-up).
5	VDD_DIFF	PWR	3.3 V power supply.
6	VSS_DIFF	GND	Ground.
7	VSS_DIFF	GND	Ground.
8	OE_DIFF2	I,PU	Active high input pin enables DIFF2 (internal 100 kΩ pull-up).

Table 6. Si53159 48-Pin QFN Descriptions

Pin #	Name	Type	Description
9	OE_DIFF3	I,PU	Active high input pin enables DIFF3 (internal 100 kΩ pull-up).
10	OE_DIFF[4:5]	I,PU	Active high input pin enables DIFF[4:5] (internal 100 kΩ pull-up).
11	OE_DIFF[6:8]	I,PU	Active high input pin enables DIFF[6:8] (internal 100 kΩ pull-up).
12	VDD_DIFF	PWR	3.3 V power supply.
13	VDD_DIFF	PWR	3.3 V power supply.
14	DIFF0	O, DIF	0.7 V, 100 MHz differential clock.
15	$\overline{\text{DIFF0}}$	O, DIF	0.7 V, 100 MHz differential clock.
16	VSS_DIFF	GND	Ground.
17	DIFF1	O, DIF	0.7 V, 100 MHz differential clock.
18	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock.
19	DIFF2	O, DIF	0.7 V, 100 MHz differential clock.
20	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock.
21	DIFF3	O, DIF	0.7 V, 100 MHz differential clock.
22	$\overline{\text{DIFF3}}$	O, DIF	0.7 V, 100 MHz differential clock.
23	VDD_DIFF	PWR	3.3V power supply.
24	VSS_DIFF	GND	Ground.
25	$\overline{\text{DIFF4}}$	O, DIF	0.7 V, 100 MHz differential clock.
26	DIFF4	O, DIF	0.7 V, 100 MHz differential clock.
27	$\overline{\text{DIFF5}}$	O, DIF	0.7 V, 100 MHz differential clock.
28	DIFF5	O, DIF	0.7 V, 100 MHz differential clock.
29	VSS_DIFF	GND	Ground.
30	$\overline{\text{DIFF6}}$	O, DIF	0.7 V, 100 MHz differential clock.
31	DIFF6	O, DIF	0.7 V, 100 MHz differential clock.
32	$\overline{\text{DIFF7}}$	O, DIF	0.7 V, 100 MHz differential clock.
33	DIFF7	O, DIF	0.7 V, 100 MHz differential clock.
34	VDD_DIFF	PWR	3.3 V power supply.
35	$\overline{\text{DIFF8}}$	O, DIF	0.7 V, 100 MHz differential clock.
36	DIFF8	O, DIF	0.7 V, 100 MHz differential clock.
37	SCLK	I	I^2C compatible SCLOCK.

Table 6. Si53159 48-Pin QFN Descriptions

Pin #	Name	Type	Description
38	SDATA	I/O	I^2C compatible SDATA.
39	CKPWRGD/PDB	I, PU	Active low input pin asserts power down (PDB) and disables all outputs (internal 100 kΩ pull-up).
40	VDD_CORE	PWR	3.3 V power supply for core.
41	DIFFIN	I	0.7 V Differential True Input, typically 100 MHz. Input frequency range 100 to 210 MHz.
42	$\overline{\text{DIFFIN}}$	O	0.7 V Differential Complement Input, typically 100 MHz. Input frequency range 100 to 210 MHz.
43	NC	NC	No connect.
44	NC	NC	No connect.
45	VSS_CORE	GND	Ground for core.
46	VSS_DIFF	GND	Ground.
47	NC	NC	No connect.
48	NC	NC	No connect.
49	GND	GND	Ground for bottom pad of the IC.

6. Ordering Guide

Part Number	Package Type	Temperature
Lead-free		
Si53159-A01AGM	48-pin QFN	Extended, –40 to 85 °C
Si53159-A01AGMR	48-pin QFN—Tape and Reel	Extended, –40 to 85 °C

7. Package Outline

Figure 4 illustrates the package details for the Si53159. Table 7 lists the values for the dimensions shown in the illustration.

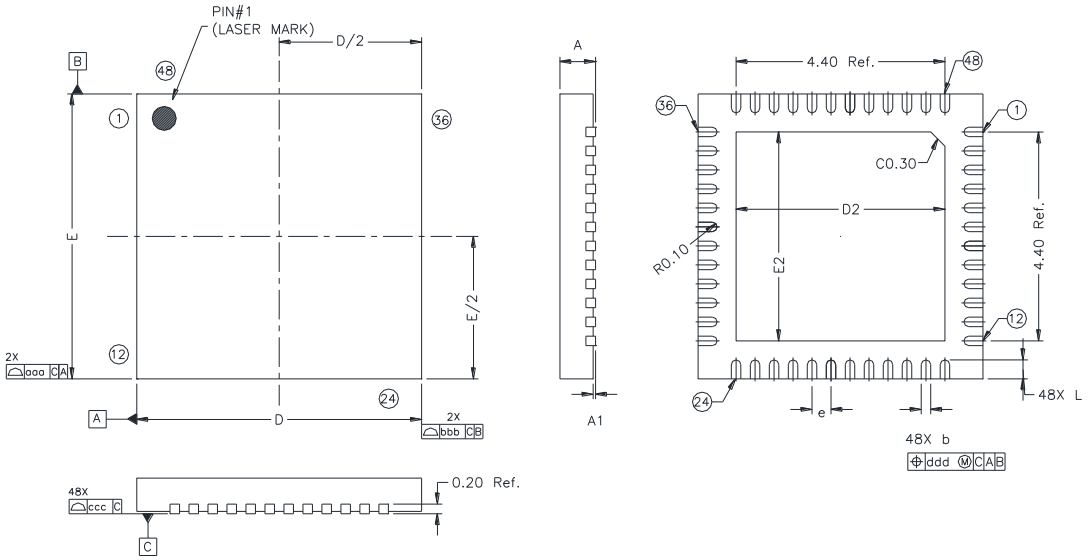


Figure 4. 48-Pin Quad Flat No Lead (QFN) Package

Table 7. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
b	0.15	0.20	0.25
D		6.00 BSC	
D2	4.30	4.40	4.50
e		0.40 BSC	
E		6.00 BSC	
E2	4.30	4.40	4.50
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.07	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components

8. Land Pattern

Figure 5 illustrates the recommended land pattern details for the Si53159 in a 48-pin QFN package. Table 8 lists the values for the dimensions shown in the illustration.

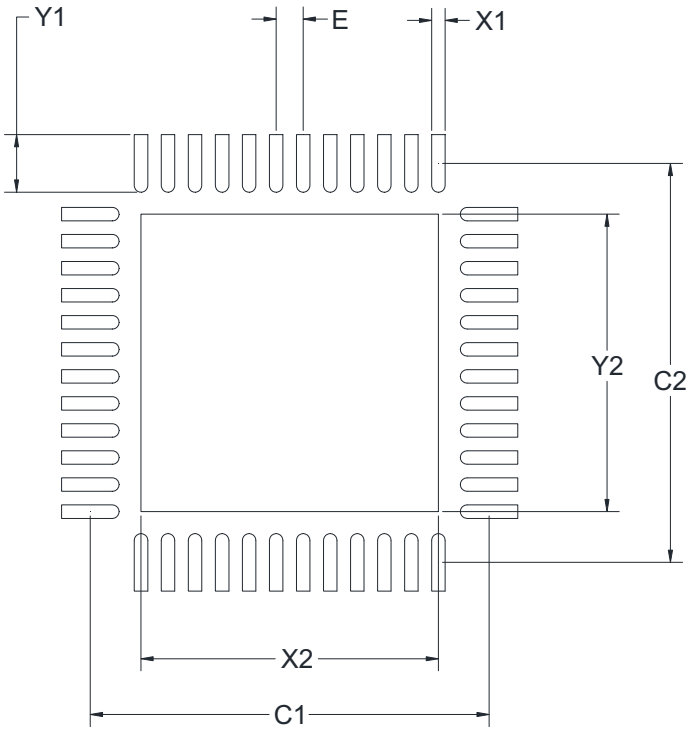


Figure 5. Land Pattern

Table 8. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	5.85	5.95
C2	5.85	5.95
X1	0.15	0.25
Y1	0.80	0.90
E	0.40 BSC	
X2	4.35	4.45
	4.35	4.45

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 4x4 array of 0.80mm square openings on 1.05mm pitch should be used for the center ground pad to achieve between 50-60% solder coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Document Change List

Revision 0.1 to Revision 1.0

- Updated Features and Description.
- Corrected pinout.
- Updated Table 2.
- Updated Section 2.1.
- Updated Section 2.1.1.
- Updated Sections 2.2 through 2.8.
- Updated Section 4.2.
- Updated Table 7.

Revision 1.0 to Revision 1.1

- Updated Features on page 1.
- Updated Description on page 1.
- Updated specs in Table 2, “AC Electrical Specifications,” on page 5.

Revision 1.1 to Revision 1.2

- Added condition for Clock Stabilization from Power-up, T_{STABLE}, in Table 2.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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